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# RTL8211F-CG RTL8211FD-CG
# RTL8211FI-CG RTL8211FDI-CG

# INTEGRATED 10/100/1000M ETHERNET PRECISION TRANSCEIVER

## DATASHEET

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## USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.0 | 2013/05/20 | First release. |
| 1.1 | 2014/04/09 | Added RTL8211FD-CG, RTL8211FI-CG, and RTL8211FDI-CG data.<br>Corrected minor typing errors. |
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| 1.5 | 2016/01/04 | Added note below Figure 4 Pin Assignments, page 6 (Due to IC size restrictions, the RTL8211FI, RTL8211FD, and RTL8211FDI do not show the 'RTL' part of the product number on the IC). |
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| 1.9 | 2018/06/11 | Revised Table 9 Power and Ground, page 10 (Pin 28).<br>Revised Table 57 Absolute Maximum Ratings, page 51 (VDD33, AVDD33).<br>Revised Table 61 DC Characteristics, page 53 (added MDC data). |

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| Revision | Release Date | Summary |
|---|---|---|
| 1.91 | 2020/07/08 | Revised Table 6 Mode Selection (Hardware Configuration), page 9 (Pins 23 & 24).<br>Revised Table 63 RGMII Timing Parameters, page 57 (Tsetup_dly & Thold_dly).<br>Revised Table 31 GBCR (1000Base-T Control Register, Address 0x09), page 37(Bit 9.8).<br>Revised Table 38 PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19), page 41(Bit 25.6).<br>Revised Table 48 MIICR2 (MII Control Register 2, Page 0xd08, Address 0x15), page 45(Bit 21.3).<br>Modify the Register Setting of Green Ethernet, page 16.<br>Added section 8.3.21 PHYCR3 (PHY Specific Control Register 3, Page 0xa44, Address 0x11), page 43.<br>Added section 8.3.23 PHYSR2 (PHY Specific Status Register 2, Page 0xa4b, Address 0x10), page 44.<br>Added section 8.3.26 MIICR1 (MII Control Register 1, Page 0xd08, Address 0x11), page 45.<br>Corrected minor typing errors. |
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# 1. General Description

The Realtek RTL8211F-CG/RTL8211FD-CG/RTL8211FI-CG/RTL8211FDI-CG is a highly integrated Ethernet transceiver that is compatible with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5 UTP cable. The RTL8211FI and RTL8211FDI are manufactured to industrial grade standards.

The RTL8211F(I)/RTL8211FD(I) uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211F(I)/RTL8211FD(I) to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) for 1000Base-T, 10Base-T, and 100Base-TX. The RTL8211F(I)/RTL8211FD(I) supports various RGMII signaling voltages, including 3.3, 2.5, 1.8, and 1.5V.

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# 2. Features

- 1000Base-T IEEE 802.3ab Compatible
- 100Base-TX IEEE 802.3u Compatible
- 10Base-T IEEE 802.3 Compatible
- Supports RGMII
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
- Built-in Wake-on-LAN (WOL)
- Supports Interrupt function
- Supports Parallel Detection
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Supports PHYRSTB core power Turn-Off
- Baseline Wander Correction
- Supports 120m for CAT.5 cable in 1000Base-T
- Selectable 3.3/2.5/1.8/1.5V signaling for RGMII
- Supports 25MHz external crystal or OSC
- Provides 125MHz clock source for MAC
- Provides 3 network status LEDs
- Supports Link Down power saving
- Green Ethernet (1000/100Mbps mode only)
- Built-in Switching Regulator and LDO
- 40-pin QFN Green Package
- 55 nm process with ultra-low power consumption
- Industrial grade manufacturing process (RTL8211FI/RTL8211FDI)

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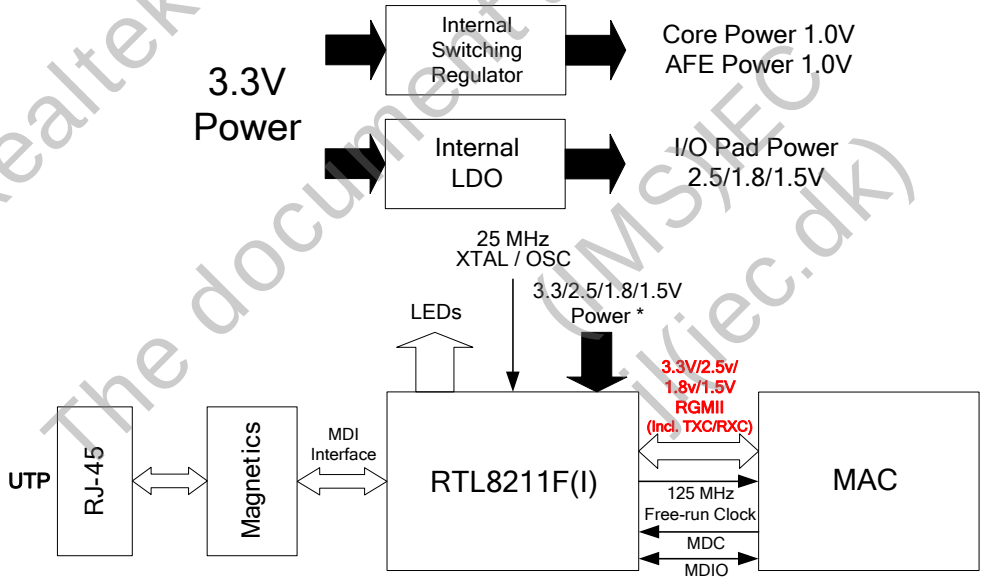
# 3. System Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch

In addition, the RTL8211F(I)/RTL8211FD(I) can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection.

## *3.1. Application Diagram - RTL8211F(I)*




**Note: 3.3/2.5/1.8/1.5V power here means I/O pad power is sourced from external power, not from the internal LDO.*

**Figure 1. Application Diagram – RTL8211F(I)**

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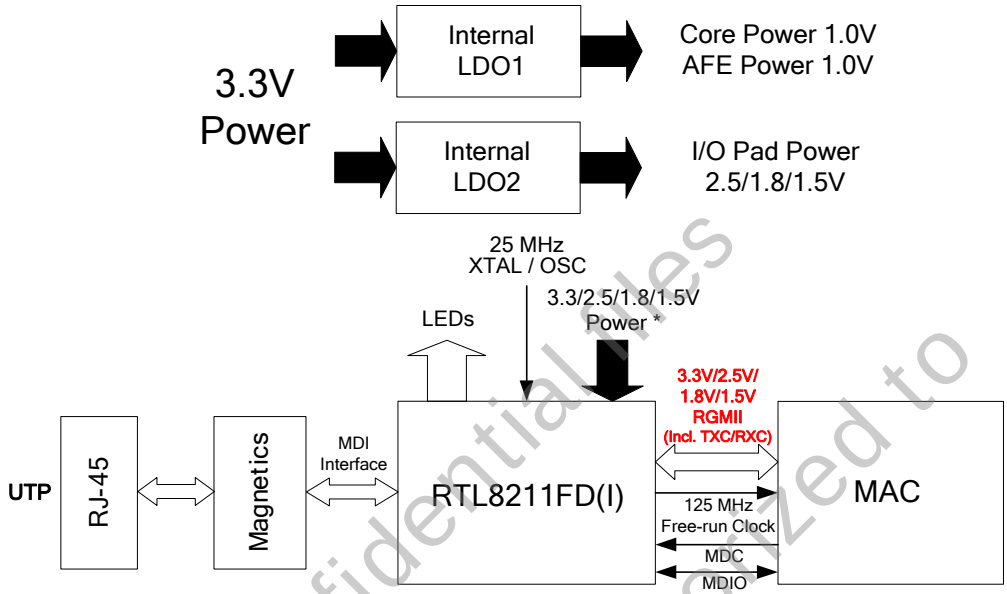
## 3.2. Application Diagram - RTL8211FD(I)




**Note: 3.3/2.5/1.8/1.5V power here means I/O pad power is sourced from external power, not from the internal LDO.*

**Figure 2. Application Diagram - RTL8211FD(I)**

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# 4. Block Diagram

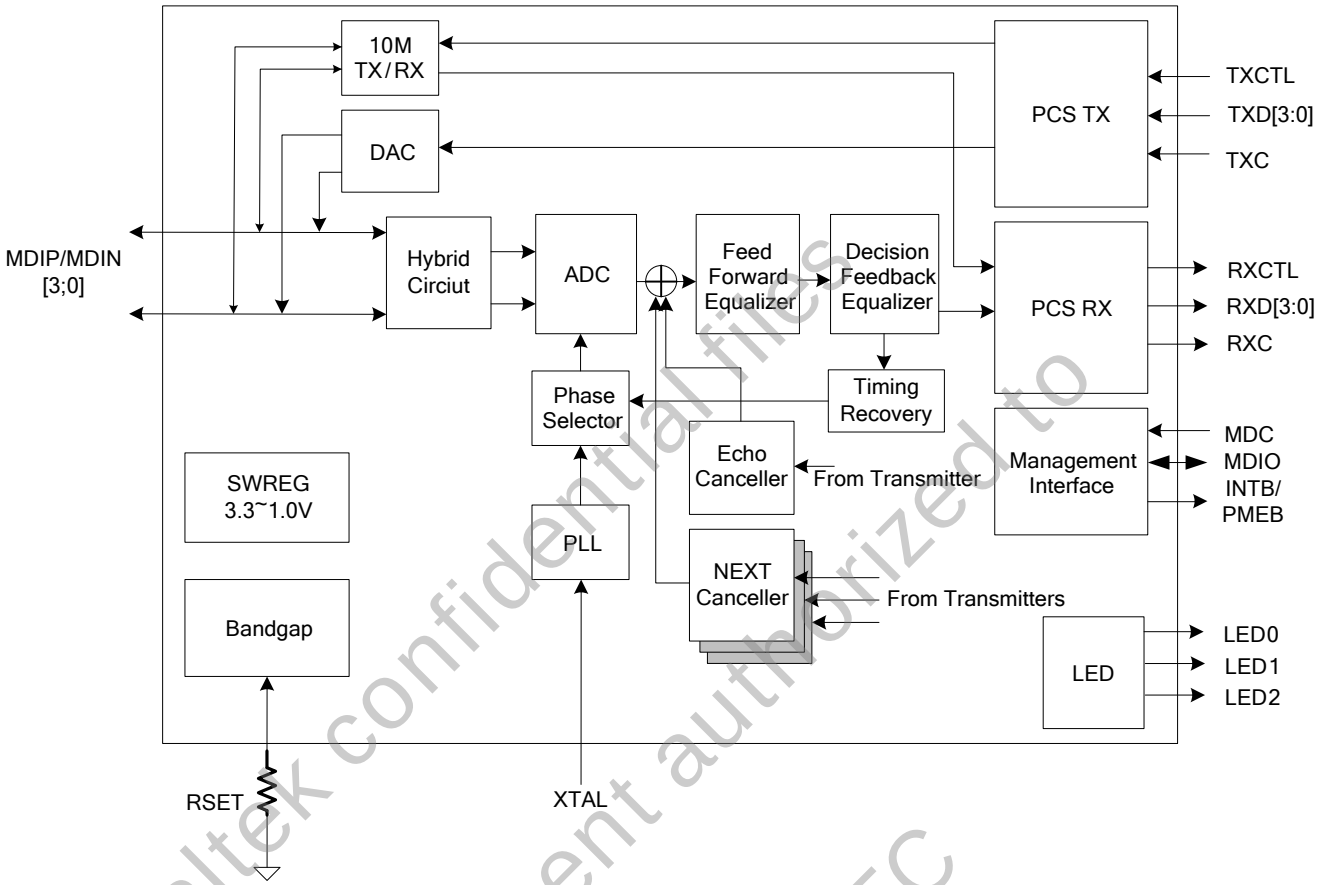


**Figure 3. Block Diagram**

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# 5. Pin Assignments

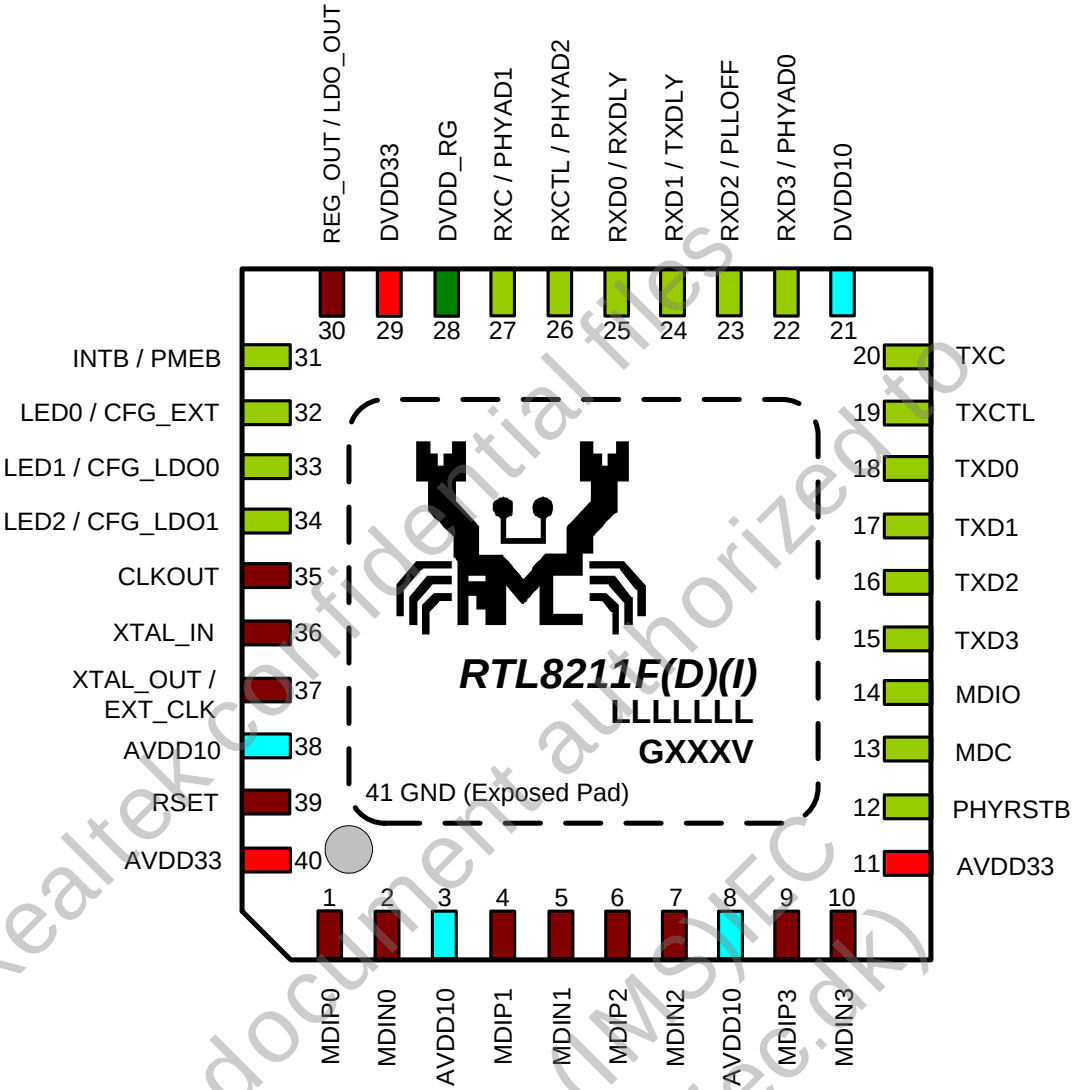


**Figure 4. Pin Assignments (40-Pin QFN)**

*Note: Due to IC size restrictions, the RTL8211FI, RTL8211FD, and RTL8211FDI do not show the 'RTL' part of the product number on the IC.*

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## 5.1. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 4).

# 6. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignments figure on page 6 for a graphical representation.

I: Input

O: Output

P: Power

PU: Internal Pull Up During Power On Reset

G: Ground

LI: Latched Input During Power up or Reset

IO: Bi-Directional Input and Output

PD: Internal Pull Down During Power On Reset

OD: Open Drain

## *6.1. Transceiver Interface*

**Table 1. Transceiver Interface**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 1 | MDIP0 | IO | In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.<br>In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| 2 | MDIN0 | IO | |
| 4 | MDIP1 | IO | In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.<br>In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| 5 | MDIN1 | IO | |
| 6 | MDIP2 | IO | In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair.<br>In MDI crossover mode, this pair acts as the BI_DD+/- pair. |
| 7 | MDIN2 | IO | |
| 9 | MDIP3 | IO | In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair.<br>In MDI crossover mode, this pair acts as the BI_DC+/- pair. |
| 10 | MDIN3 | IO | |

*Note: BI_DA+/-, BI_DB+/-, BI_DC+/-, BI_DD+/- means the logical wire-pairs as described in section 40.1.3 of the IEEE 802.3 standard.*

## *6.2. Clock*

**Table 2. Clock**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 36 | XTAL_IN | I | 25MHz Crystal Input.<br>Connect to GND if an external 25MHz oscillator drives XTAL_OUT/EXT_CLK. |
| 37 | XTAL_OUT/<br>EXT_CLK | O | 25MHz Crystal Output.<br>If a 25MHz oscillator is used, connect XTAL_OUT/EXT_CLK to the oscillator's output (see section 10.3, page 52 for clock source specifications). |
| 35 | CLKOUT | O | 125/25MHz Reference Clock Generated from Internal PLL.<br>This pin should be kept floating if this clock is not used by MAC. |

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## 6.3. RGMII

**Table 3. RGMII**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 20 | TXC | I | The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed. |
| 18 | TXD0 | I | Transmit Data.<br>Data is transmitted from MAC to PHY via TXD[3:0]. |
| 17 | TXD1 | I | |
| 16 | TXD2 | I | |
| 15 | TXD3 | I | |
| 19 | TXCTL | I | Transmit Control Signal from the MAC. |
| 27 | RXC | O/LI/PD | The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. |
| 25 | RXD0 | O/LI/PU | Receive Data.<br>Data is transmitted from PHY to MAC via RXD[3:0]. |
| 24 | RXD1 | O/LI/PD | |
| 23 | RXD2 | O/LI/PD | |
| 22 | RXD3 | O/LI/PU | |
| 26 | RXCTL | O/LI/PD | Receive Control Signal to the MAC. |

## 6.4. Management Interface

**Table 4. Management Interface**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 13 | MDC | I | Management Data Clock. |
| 14 | MDIO | IO/PU | Input/Output of Management Data.<br>Pull up 3.3/2.5/1.8/1.5V for 3.3/2.5/1.8/1.5V I/O, respectively. |
| 31 | INTB/PMEB | O/OD | This pin is shared by two functions, keep this pin floating if either of the functions is not used.<br>1. Interrupt (supports 3.3V pull up).<br>Set low if the specified events happened; active low.<br>2. Power Management Event (supports 3.3V pull up).<br>Set low if received a magic packet or Wake-Up frame, or wake up event; active low.<br>*Note 1: The behavior of this pin is level-triggered.*<br>*Note 2: The function of this pin (INTB/PMEB) can be assigned by Page 0xd40, Reg.22, bit[5]:*<br>*1: Pin 31 functions as PMEB*<br>*0: Pin 31 functions as INTB (default)*<br>*Note 3: For more detailed INTB/PMEB usage, see section 7.6, page 13.* |

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## 6.5. Reset

**Table 5. Reset**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 12 | PHYRSTB | I/PU | Hardware Reset. Active low.<br>For a complete PHY reset, this pin must be asserted low for at least 10ms.<br>All registers will be cleared after a hardware reset. |

*Note: See section 7.17, page 28 for more details.*

## 6.6. Mode Selection (Hardware Configuration)

**Table 6. Mode Selection (Hardware Configuration)**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 22 | PHYAD0 | O/LI/PU | PHYAD[2:0]:<br>PHY Address Configuration. |
| 27 | PHYAD1 | O/LI/PD | |
| 26 | PHYAD2 | O/LI/PD | |
| 23 | PLLOFF | O/LI/PD | ALDPS Mode PLL Off Configuration.<br>Pull up to stop PLL when entering ALDPS mode.<br>*Note:*<br>*Whole system power consumption in typical ALDPS mode is 43.8mW for the RTL8211F(I), and 58mW for the RTL8211FD(I).*<br>*Whole system power consumption in ALDPS low power mode (with PLL turned off) is 17mW for the RTL8211F(I), and 26.8 mW for the RTL8211FD(I).*<br>*All with 1.8V RGMII.* |
| 24 | TXDLY | O/LI/PD | RGMII Transmit Clock Timing Control.<br>Pull up to enable PHY internal TXC delay. |
| 25 | RXDLY | O/LI/PU | RGMII Receiver Clock Timing Control.<br>Pull up to add 2ns delay to RXC for RXD latching. |
| 32 | CFG_EXT | O/LI/PD | I/O Pad External Power Source Mode Configuration.<br>Pull up to use the external power source for the I/O pad.<br>Pull down to use the integrated LDO to transform the desired voltage for the I/O pad. |
| 33 | CFG_LDO0 | O/LI/PU | CFG_LDO[1:0]:<br>LDO Output Voltage Selection for the RGMII I/O Pad/<br>External Power Source Voltage Selection for the RGMII I/O Pad.<br>When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad:<br>2'b00: Reserved<br>2'b01: 2.5V<br>2'b10: 1.8V<br>2'b11: 1.5V<br>When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of the external power for IO pad:<br>2'b00: 3.3V<br>2'b01: 2.5V<br>2'b10: 1.8V<br>2'b11: 1.5V |
| 34 | CFG_LDO1 | O/LI/PD | |

*Note: For more information, see section 7.8, Hardware Configuration, page 14.*

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## 6.7. LED Default Settings

**Table 7. LED Default Settings**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 32 | LED0 | O/LI/PD | High = Link Up at 10Mbps<br>Blinking = Transmitting or Receiving. |
| 33 | LED1 | O/LI/PU | Low = Link Up at 100Mbps<br>Blinking = Transmitting or Receiving. |
| 34 | LED2 | O/LI/PD | High = Link Up at 1000Mbps<br>Blinking = Transmitting or Receiving. |

*Note 1: High/Low active depends on hardware configuration setting (see section 7.9, page 15).*
*Note 2: See section 7.14 LED Configuration, page 25 for more LED setting details.*

## 6.8. Regulator and Reference

**Table 8. Regulator and Reference**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 39 | RSET | O | Reference (External Resistor Reference). |
| 30 | REG_OUT<br>(RTL8211F(I))<br>LDO_OUT<br>(RTL8211FD(I)) | O | For RTL8211F(I):<br>Switching Regulator 1.0V Output. Connect to a 2.2µH or 4.7µH inductor.<br>For RTL8211FD(I):<br>Low-dropout Regulator 1.0V Output. |

## 6.9. Power and Ground

**Table 9. Power and Ground**

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 29 | DVDD33 | P | Digital non-RGMII I/O Power. 3.3V. |
| 28 | DVDD_RG | P | Digital RGMII I/O, MDIO, MDC Pad Power.<br>When pulling high the CFG_EXT pin during Hardware Configuration (External Power mode), connect this pin to the external power source for 3.3/2.5/1.8/1.5V RGMII I/O pads. |
| 21 | DVDD10 | P | Digital Core Power. 1.0V. |
| 11, 40 | AVDD33 | P | Analog Power. 3.3V. |
| 3, 8, 38 | AVDD10 | P | Analog Power. 1.0V. |
| 41 | GND | G | Ground.<br>Exposed Pad (E-Pad) is Analog and Digital Ground (see section 11 Mechanical Dimensions, page 58). |

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# 7. Function Description

## 7.1. Transmitter

### 7.1.1. 1000Mbps Mode

The RTL8211F(I)/RTL8211FD(I)'s PCS layer receives data bytes from the MAC through the RGMII interface and performs generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5 cable at 125MBaud/s through a D/A converter.

### 7.1.2. 100Mbps Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXCLK), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

### 7.1.3. 10Mbps Mode

The transmit 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXCLK), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

## 7.2. Receiver

### 7.2.1. 1000Mbps Mode

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the RGMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive RGMII interface and sends it to the Rx Buffer Manager.

### 7.2.2. 100Mbps Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the RGMII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

### 7.2.3. 10Mbps Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder, and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the RGMII interface at a clock speed of 2.5MHz.

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## 7.3. Energy Efficient Ethernet (EEE)

The RTL8211F(I)/RTL8211FD(I) supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

Refer to http://www.ieee802.org/3/az/index.html for more details.

## 7.4. Wake-On-LAN (WOL)

The RTL8211F(I)/RTL8211FD(I) can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs[1]. The system can then be restored to a normal state to process incoming jobs. The PMEB pin needs to be connected with a 4.7k-ohm resistor and pulled up to 3.3V. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the PMEB pin will be set low to notify the system to wake up. Refer to the RTL8211F_Series_WOL_App_Note for details.

Magic Packet Wake-up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8211F(I)/RTL8211FD(I), e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8211F(I)/RTL8211FD(I)
- The received Magic Packet does not contain a CRC error
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8211F(I)/RTL8211FD(I), e.g., a broadcast, multicast, or unicast address to the current RTL8211F(I)/RTL8211FD(I)
- The received Wake-Up Frame does not contain a CRC error
- The 16-bit CRC[2] of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8211F(I)/RTL8211FD(I) is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet. Non-specific packets are also supported

*Note 1: The INTB and PMEB functions share the same pin (pin 31), and can be determined by Page 0xd40, Reg.22, bit[5].*

*Note 2: 16-bit CRC: The RTL8211F(I)/RTL8211FD(I) supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial =* $x^{16}+x^{12}+x^{5}+1$.

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## 7.5. Interrupt

The RTL8211F(I)/RTL8211FD(I) provides an active low interrupt output pin (INTB) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register INSR (section 8.3.19 INSR (Interrupt Status Register, Page 0xa43, Address 0x1D), page 42).

The interrupts can be individually enabled or disabled by setting or clearing bits in the interrupt enable register INER (section 8.3.15 INER (Interrupt Enable Register, Page 0xa42, Address 0x12), page 39). When an enabled interrupt condition occurs, the interrupt pin is driven low, and the interrupts can be self-cleared (INTB pin de-asserted) by reading the corresponding interrupt status registers through MDC/MDIO interface.

*Note 1: The interrupt of the RTL8211F(I)/RTL8211FD(I) is a level-triggered mechanism.*
*Note 2: The INTB and PMEB functions share the same pin (pin 31), and can be determined by Page 0xd40, Reg.22, bit[5].*

## 7.6. INTB/PMEB Pin Usage

The INTB/PMEB pin (pin 31) of the RTL8211F(I)/RTL8211FD(I) is designed to notify in cases of both interrupt and WOL events. The default mode of this pin is INTB (Page 0xd40, Reg.22, bit[5] = 0). For general use, indication of a WOL event is also integrated into one of the interrupt events (Page 0, Reg 18, bit[7]), which would be triggered when any specified WOL event occurs. However, the 'Pulse Low' waveform format is not supported during this mode; only the Active Low, level-triggered waveform is provided. Refer to section 6.1 in the RTL8211F_Series_WOL_App_Note for more information.

If PMEB mode is selected (Page 0xd40, Reg.22, bit[5] = 1), pin 31 becomes a fully functional PMEB pin. Note that the interrupt function is disabled in this mode.

## 7.7. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors to reduce BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs MDI0 and MDI1 are used.

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## 7.8. Hardware Configuration

The I/O pad voltage, interface mode, and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 10. To set the CONFIG pins, an external pull-high or pull-low via resistor is required.

**Table 10. CONFIG Pins vs. Configuration Register**

| CONFIG Pin | Configuration |
|---|---|
| RXD3 | PHYAD[0] |
| RXC | PHYAD[1] |
| RXCTL | PHYAD[2] |
| RXD2 | PLLOFF |
| RXD1 | TXDLY |
| RXD0 | RXDLY |
| LED0 | CFG_EXT |
| LED1 | CFG_LDO[0] |
| LED2 | CFG_LDO[1] |

**Table 11. Configuration Register Definitions**

| Configuration | Description |
|---|---|
| PHYAD[2:0] | PHY Address.<br>PHYAD sets the PHY address for the device. The RTL8211F(I)/RTL8211FD(I) supports PHY addresses from 0x01 to 0x07.<br>*Note 1: An MDIO command with PHY address = 0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xa43, Reg24, bit[13 ]= 0 (See section 8.3.16, page 40).*<br>*Note 2: The RTL8211F(I)/RTL8211FD(I) with PHYAD[2:0] = 000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xa43, Reg24, bit[6] = 1 (See section 8.3.16, page 40).* |
| PLLOFF | ALDPS Mode PLL Off Configuration.<br>1: Stop PLL when entering ALDPS mode (via 4.7k-ohm to DVDD_RG)<br>0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND) |
| TXDLY | RGMII Transmit Clock Timing Control.<br>1: Add 2ns delay to TXC for TXD latching (via 4.7k-ohm to DVDD_RG)<br>0: No delay (via 4.7k-ohm to GND) |
| RXDLY | RGMII Receive Clock Timing Control.<br>1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG)<br>0: No delay (via 4.7k-ohm to GND) |
| CFG_EXT | RGMII I/O Pad External Power Source Mode Configuration.<br>1: Use the external power source for the RGMII I/O pad (via 4.7k-ohm to 3.3V)<br>0: Use the integrated LDO to transform the desired voltage for the RGMII I/O pad (via 4.7k-ohm to GND) |

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| Configuration | Description |
|---|---|
| CFG_LDO[1:0] | LDO Output Voltage Selection for the RGMII I/O pad/<br>External Power Source Voltage Selection for the RGMII I/O pad.<br>When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for the RGMII I/O pad: (via 4.7k-ohm to GND)<br>00: Reserved<br>01: 2.5V<br>10: 1.8V<br>11: 1.5V<br>When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for external power voltage selection for the RGMII I/O pad: (via 4.7k-ohm to 3.3V)<br>00: 3.3V<br>01: 2.5V<br>10: 1.8V<br>11: 1.5V |

## 7.9. LED and LDO Configuration

In order to reduce the pin count on the RTL8211F(I)/RTL8211FD(I), the LED pins are duplexed with the CFG_EXT and CFG_LDO[1:0] pins. As the Hardware Configuration shares the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding CFG_EXT/CFG_LDO[1:0] inputs upon power-on/reset.

For example, as Figure 5 (left-side) shows, if a given CFG_EXT/CFG_LDO[1:0] inputs are resistively pulled high then the corresponding LED outputs will be configured as an active low driver. On the right side, we can see that if a given CFG_EXT/CFG_LDO[1:0] inputs are resistively pulled low then the corresponding output will be configured as an active high driver. The Hardware Configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.

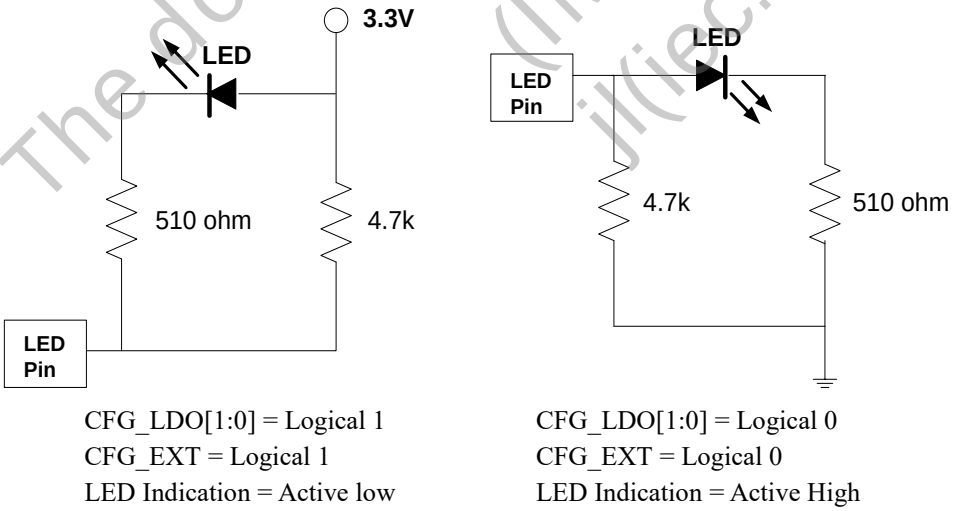


**Figure 5. LED and LDO Configuration**

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# *7.10. Green Ethernet (1000/100Mbps Mode Only)*

## 7.10.1. Cable Length Power Saving

In 1000/100Mbps mode the RTL8211F(I)/RTL8211FD(I) provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides intermediate performance with minimum power consumption.

## 7.10.2. Register Setting

**Follow the register settings below to DISABLE Green Ethernet (Default is 'Enabled')**

Write Page 0x0B82 reg16 = 0x0010

Waiting for Page 0x0B80 reg16 bit [6] = 1 ( or delay 200ms)

Write Page 0x0A43 reg27 = 0x8146

Write Page 0x0A43 reg28 = 0x9501

Write Page 0x0B82 reg23 = 0x0001

Write Page 0x0A43 reg27 = 0x8011

Write Page 0x0A43 reg28 = 0x573f

Write Page 0x0A43 reg27 = 0x0000

Write Page 0x0A43 reg28 = 0x0000

Write Page 0x0B82 reg23 = 0x0000

Write Page 0x0A43 reg27 = 0x8146

Write Page 0x0A43 reg28 = 0x0000

Write Page 0x0B82 reg16 = 0x0000

**Follow the register settings below to ENABLE Green Ethernet (Default is 'Enabled')**

Write Page 0x0B82 reg16 = 0x0010

Waiting for Page 0x0B80 reg16 bit [6] = 1 ( or delay 200ms)

Write Page 0x0A43 reg27 = 0x8146

Write Page 0x0A43 reg28 = 0x9501

Write Page 0x0B82 reg23 = 0x0001

Write Page 0x0A43 reg27 = 0x8011

Write Page 0x0A43 reg28 = 0xd73f

Write Page 0x0A43 reg27 = 0x0000

Write Page 0x0A43 reg28 = 0x0000

Write Page 0x0B82 reg23 = 0x0000

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Write Page 0x0A43 reg27 = 0x8146

Write Page 0x0A43 reg28 = 0x0000

Write Page 0x0B82 reg16 = 0x0000

## *7.11. MAC/PHY Interface*

The RTL8211F(I)/RTL8211FD(I) supports industry standards and is suitable for most off-the-shelf MACs with an RGMII interface.

### 7.11.1. RGMII

Among the RGMII interface in 100Base-TX and 10Base-T modes, TXC and RXC sources are 25MHz and 2.5MHz respectively; while in 1000Base-T mode, TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on the rising and falling edge of the clock.

### 7.11.2. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

The RTL8211F(I)/RTL8211FD(I) can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the management registers, see section 8 Register Descriptions, page 29.

**Table 12. Management Frame Format**

| | Management Frame Fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Preamble | ST | OP | PHYAD | REGAD | TA | DATA | IDLE |
| Read | 1…1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| Write | 1…1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

**Table 13. Management Frame Description**

| Name | Description |
|---|---|
| Preamble | 32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC.<br>This provides synchronization for the PHY. |
| ST | Start of Frame.<br>Indicated by a 01 pattern. |
| OP | Operation Code.<br>Read: 10<br>Write: 01 |
| PHYAD | PHY Address.<br>Up to eight PHYs can be connected to one MAC. This 3-bit field selects which PHY the frame is directed to. |

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| Name | Description |
|---|---|
| REGAD | Register Address.<br>This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to. |
| TA | Turnaround.<br>This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction. |
| DATA | Data. These are the 16 bits of data. |
| IDLE | Idle Condition.<br>Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'. |

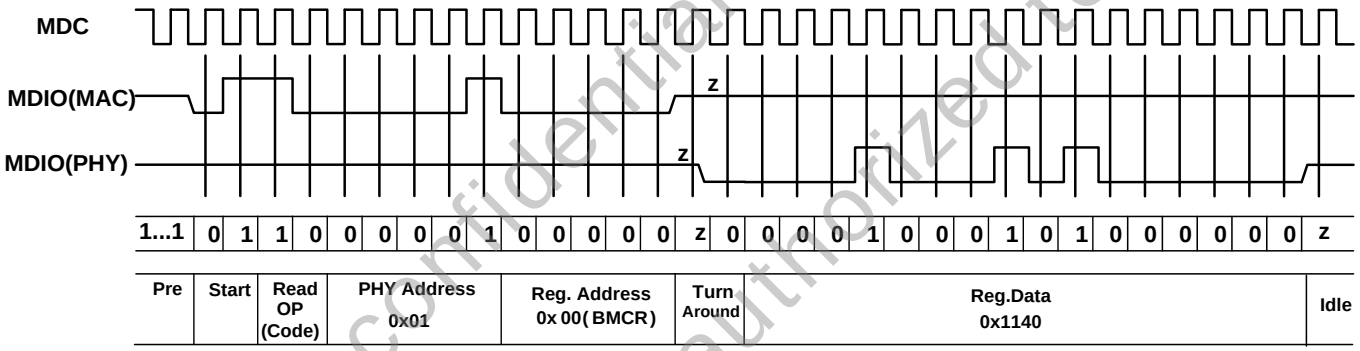


**Figure 6. MDC/MDIO Read Timing**

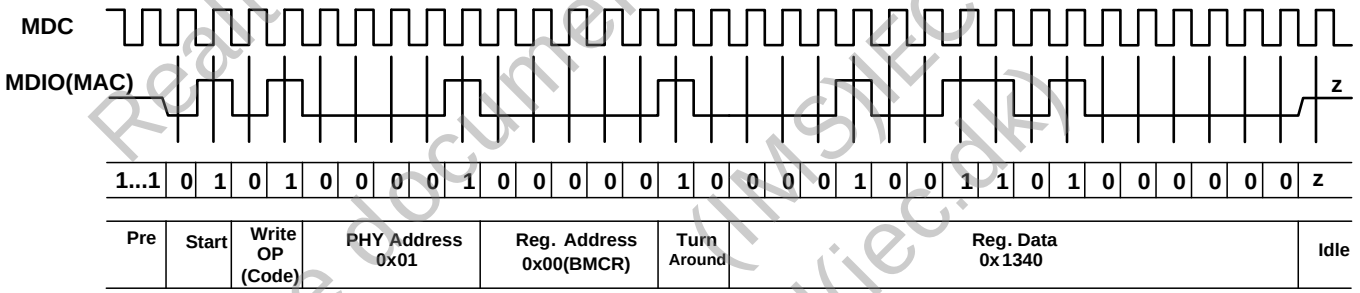


**Figure 7. MDC/MDIO Write Timing**

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### 7.11.3. Change Page

Set MDIO commands as shown below in order to switch to the desired Page 0xXYZ (in Hex).

1. Write Register 31 Data = 0x0XYZ (Page 0xXYZ)

2. Read/Write the target Register Data

3. Write Register 31 Data = 0x0000 or 0xa42 (switch back to IEEE Standard Registers)

### 7.11.4. Access to MDIO Manageable Device (MMD)

The MDIO Manageable Device (MMD) is an extension to the management interface that provides the ability to access more device registers while still retaining logical compatibility with the MDIO interface, defined in section 8.2 MMD Register Mapping and Definitions, page 30. Access to MMD configuration is provided via Registers 13 and 14.

**MMD Read/Write Operation**

1. Write Function field to 00 (address mode) and DEVAD field to the device address value for the desired MMD (Register 13).

2. Write the desired address value to the MMD's address register (Register 14).

3. Write Function field to 01 (data mode; no post increment) and DEVAD field to the same device address for the desired MMD (Register 13).

4. Read: Go to step 5. Write: Go to step 6.

5. Read the content of the selected register in MMD (Register 14).

6. Write the content of the selected register in MMD (Register 14).

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## 7.12. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

- Auto-Negotiation Priority Resolution
- Auto-Negotiation Master/Slave Resolution
- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution
- Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211F(I)/RTL8211FD(I) can be configured to have auto-negotiation enabled, or be set to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the ANAR and GBCR register (register 4 and 9).

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up
- Hardware reset
- Software reset (register 0.15)
- Restart auto-negotiation (register 0.9)
- Transition from power down to power up (register 0.11)
- Entering the link fail state

**Table 14. 1000Base-T Base and Next Page Bit Assignments**

| Bit | Name | Bit Description | Register Location |
|---|---|---|---|
| | | **Base Page** | |
| D15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| D14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| D13 | RF | Remote Fault.<br>1: Indicates to its link partner that a device has encountered a fault condition | - |
| D[12:5] | A[7:0] | Technology Ability Field.<br>Indicates to its link partner the supported technologies specific to the selector field value. | Register 4.[12:5]<br>Table 26, page 34. |
| D[4:0] | S[4:0] | Selector Field.<br>Always 00001.<br>Indicates to its link partner that it is an IEEE 802.3 device. | Register 4.[4:0]<br>Table 26, page 34. |

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| Bit | Name | Bit Description | Register Location |
|---|---|---|---|
| **PAGE 0 (Message Next Page)** | | | |
| M15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| M14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| M13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page | - |
| M12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message | - |
| M11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| M[10:0] | - | 1000Base-T Message Code (Always 8). | - |
| **PAGE 1 (Unformatted Next Page)** | | | |
| U15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| U14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| U13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page | - |
| U12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message | - |
| U11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| U[10:5] | - | Reserved. Transmit as 0. | - |
| U4 | - | 1000Base-T Half Duplex.<br>1: Half duplex 0: No half duplex | - |
| U3 | - | 1000Base-T Full Duplex.<br>1: Full duplex 0: No full duplex | - |
| U2 | - | 1000Base-T Port Type Bit.<br>1: Multi-port device 0: Single-port device | Register 9.10 (GBCR)<br>Table 31, page 37. |
| U1 | - | 1000Base-T Master-Slave Manual Configuration Value.<br>1: Master 0: Slave<br>This bit is ignored if bit 9.12 = 0 | Register 9.11 (GBCR)<br>Table 31, page 37. |
| U0 | - | 1000Base-T Master-Slave Manual Configuration Enable.<br>1: Manual Configuration Enable<br>This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11 | Register 9.12 (GBCR)<br>Table 31, page 37. |

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| Bit | Name | Bit Description | Register Location |
|---|---|---|---|
| **PAGE 2 (Unformatted Next Page)** | | | |
| U15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| U14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| U13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page | - |
| U12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message | - |
| U11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| U[10:0] | - | 1000Base-T Master-Slave Seed Bit[10:0] | Master-Slave Seed Value SB[10:0] |

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### 7.12.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1. 1000Base-T Full Duplex (highest priority)
2. 1000Base-T Half Duplex
3. 100Base-TX Full Duplex
4. 100Base-TX Half Duplex
5. 10Base-T Full Duplex
6. 10Base-T Half Duplex (lowest priority)

### 7.12.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority
  - Multi-port > Single-port
  - Manual > Non-manual
- Determination of Master/Slave configuration from LCW
  - Manual_MASTER = U0*U1
  - Manual_SLAVE = U0*!U1
  - Single-port device = !U0*!U2
  - Multi-port device = !U0*U2

    Where: U0 is bit 0 of the Unformatted Page 1
    U1 is bit 1 of the Unformatted Page 1
    U2 is bit 2 of the Unformatted Page 1
- Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master
- Master-Slave configuration process resolution:
  - Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution
  - Unsuccessful: Auto-Negotiation restarts
  - Fault Detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed

### 7.12.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 26, page 34). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 27, page 35). A PHY layer device such as the RTL8211F(I)/RTL8211FD(I) is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

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## 7.13. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two computers connected to each other with a CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8211F(I)/RTL8211FD(I) is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211F(I)/RTL8211FD(I) advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If set to half duplex, then only half duplex is advertised.
2. If set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disable by setting (Page 0xa43, Reg 24, bit[9:8]) manually, see section 8.3.16, page 40.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via register 0.12, speed via registers 0.13, 0.6, and duplex via register 0.8. The abilities that are advertised can be changed via registers 4 and 9. Changes to registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

- Software reset (register 0.15)
- Restart of Auto-Negotiation (register 0.9)
- Transition from power-down to power-up (register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3). Hence a write into register 4 or 9 has no effect once the RTL8211F(I)/RTL8211FD(I) begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211F(I)/RTL8211FD(I) completes Auto-Negotiation, it updates the various statuses in registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in Page 0xa43, Reg 26 and 29 (Reg 29 is valid after enabling the interrupts in Page 0xa42, Reg 18).

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# 7.14. LED Configuration

## 7.14.1. Customized LED Function

The RTL8211F(I)/RTL8211FD(I) supports three LED pins, suitable for multiple types of applications that can directly drive the LEDs. The output of these pins is determined by setting the corresponding bits in Page 0xd04 Register 16. The functionality of the RTL8211F(I)/RTL8211FD(I) LEDs is shown in Table 15.

**Table 15. LED Default Definitions**

| Pin | Description |
|---|---|
| LED0 | 10M Link and Active (Transmitting or Receiving). |
| LED1 | 100M Link and Active (Transmitting or Receiving). |
| LED2 | 1000M Link and Active (Transmitting or Receiving). |

The LED pins can be customized from Page 0xd04 Register 16. To change the register page, see note (below) and Table 16 LED Register Table. Two LED configuration modes are provided by the RTL8211F(I)/RTL8211FD(I), each with 16 configuration types (see Table 17 LED Configuration Table – Mode A, and Table 18 LED Configuration Table – Mode B, page 26). To switch between these two modes, set Page 0xd04, Reg 16, bit[15] to 0 (Mode A) or 1 (Mode B).

*Note: To switch to Page 0xd04, set Register 31 Data = 0x0d04 (set page). After LED setting, switch back to the PHY's IEEE Standard Registers, i.e. Page 0 or Page 0xa42 (Register 31 Data = 0 or 0xa42).*

**Table 16. LED Register Table**

| | LINK Speed | | | Active (Tx/Rx) |
|---|---|---|---|---|
| | 10Mbps | 100Mbps | 1000Mbps | |
| LED0 | Reg16 Bit0 | Reg16 Bit1 | Reg16 Bit3 | Reg16 Bit4 |
| LED1 | Reg16 Bit5 | Reg16 Bit6 | Reg16 Bit8 | Reg16 Bit9 |
| LED2 | Reg16 Bit10 | Reg16 Bit11 | Reg16 Bit13 | Reg16 Bit14 |

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**Table 17. LED Configuration Table – Mode A**

| Pin | LINK Bit | | | Active (TX/RX) Bit | Description |
|---|---|---|---|---|---|
| | 10Mbps | 100Mbps | 1000Mbps | | |
| LED0<br>LED1<br>LED2 | 0 | 0 | 0 | 0 | N/A.<br>*Note: No LPI mode for this setting* |
| | 0 | 0 | 0 | 1 | N/A.<br>*Note: No LPI mode for this setting* |
| | 0 | 0 | 1 | 0 | Link 1000 |
| | 0 | 0 | 1 | 1 | Link 1000+Active 1000 |
| | 0 | 1 | 0 | 0 | Link 100 |
| | 0 | 1 | 0 | 1 | Link 100+Active 100 |
| | 0 | 1 | 1 | 0 | Link 100/1000 |
| | 0 | 1 | 1 | 1 | Link 100/1000+Active 100/1000 |
| | 1 | 0 | 0 | 0 | Link 10 |
| | 1 | 0 | 0 | 1 | Link 10+Active 10 |
| | 1 | 0 | 1 | 0 | Link 10/1000 |
| | 1 | 0 | 1 | 1 | Link 10/1000+Active 10/1000 |
| | 1 | 1 | 0 | 0 | Link 10/100 |
| | 1 | 1 | 0 | 1 | Link 10/100+Active 10/100 |
| | 1 | 1 | 1 | 0 | Link 10/100/1000 |
| | 1 | 1 | 1 | 1 | Link 10/100/1000+Active 10/100/1000 |

**Table 18. LED Configuration Table – Mode B**

| Pin | LINK Bit | | | Active (TX/RX) Bit | Description |
|---|---|---|---|---|---|
| | 10Mbps | 100Mbps | 1000Mbps | | |
| LED0<br>LED1<br>LED2 | 0 | 0 | 0 | 0 | N/A.<br>*Note: No LPI mode for this setting* |
| | 0 | 0 | 0 | 1 | Active 10/100/1000<br>*Note: No LPI mode for this setting* |
| | 0 | 0 | 1 | 0 | Link 1000 |
| | 0 | 0 | 1 | 1 | Link 1000+ Active 10/100/1000 |
| | 0 | 1 | 0 | 0 | Link 100 |
| | 0 | 1 | 0 | 1 | Link 100+ Active 10/100/1000 |
| | 0 | 1 | 1 | 0 | Link 100/1000 |
| | 0 | 1 | 1 | 1 | Link 100/1000+ Active 10/100/1000 |
| | 1 | 0 | 0 | 0 | Link 10 |
| | 1 | 0 | 0 | 1 | Link 10+ Active 10/100/1000 |
| | 1 | 0 | 1 | 0 | Link 10/1000 |
| | 1 | 0 | 1 | 1 | Link 10/1000+ Active 10/100/1000 |
| | 1 | 1 | 0 | 0 | Link 10/100 |
| | 1 | 1 | 0 | 1 | Link 10/100+ Active 10/100/1000 |
| | 1 | 1 | 1 | 0 | Link 10/100/1000 |
| | 1 | 1 | 1 | 1 | Link 10/100/1000+Active 10/100/1000 |

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### 7.14.2. EEE LED Function

EEE Idle mode: LED continuous slow blinking.

EEE Active mode: LED fast and slow blinking (on packet transmitting and receiving).

Refer to section 8.3.25, page 44 for EEE LED enable setting.

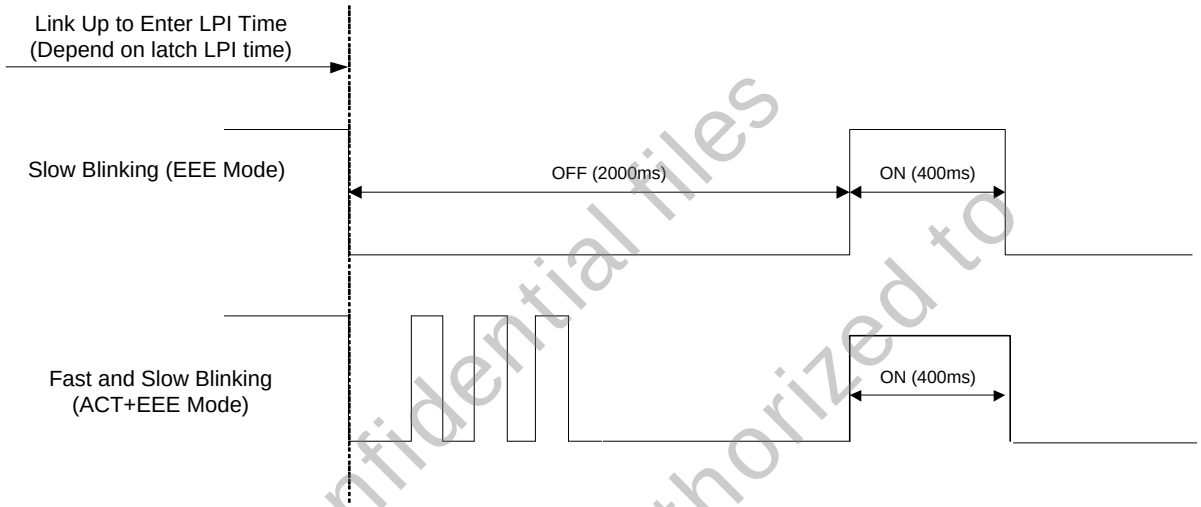


**Figure 8. EEE LED Behavior**

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## 7.15. Polarity Correction

The RTL8211F(I)/RTL8211FD(I) automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

## 7.16. Power

A voltage regulator is implemented to generate operating power (switching regulator for the RTL8211F(I); LDO for the RTL8211FD(I)). The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211F(I)/RTL8211FD(I) converts the 3.3V steady power source to 1.0V via a switching regulator/LDO.

The RTL8211F(I)/RTL8211FD(I) implements an option for the RGMII power pins. The standard I/O voltage of the RGMII interface is 3.3V, with support for 2.5/1.8/1.5V to lower EMI. The 2.5/1.8/1.5V power source for RGMII is supplied from an internal LDO or from an external power source.

## 7.17. PHY Reset (Hardware Reset)

The RTL8211F(I)/RTL8211FD(I) has a PHYRSTB pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (Tgap in Figure 9) for the internal regulator. Wait for at least 72ms* (for internal circuits settling time) before accessing the PHY register. All registers will return to default values after a hardware reset.

** Note: Not included the 1.0V rise time. Refer to Note 6 in section 9.3, page 49, and the RTL8211F_Series_Power_Sequence_App_Note for more detailed information.*

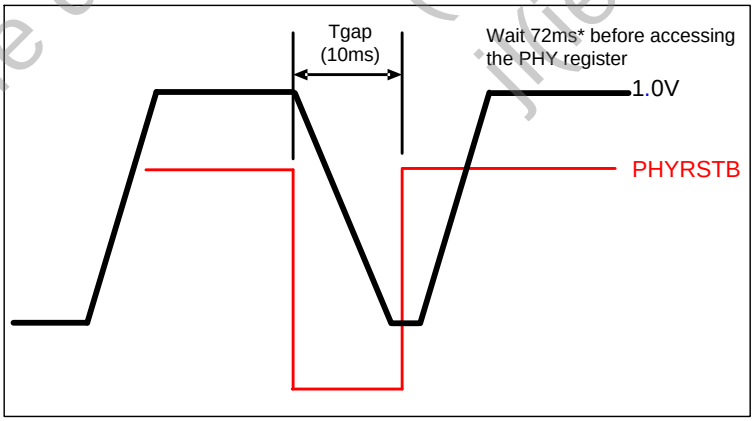


**Figure 9. PHY Reset Timing**

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# 8. Register Descriptions

## 8.1. Register Mapping and Definitions

**Table 19. Register Access Types**

| Type | Description |
|---|---|
| LH | Latch high. If the status is high, this field is set to '1' and remains set. |
| RC | Read-cleared. The register field is cleared after read. |
| RO | Read only. |
| RW | Read and Write |
| SC | Self-cleared. Writing a '1' to this register field causes the function to be activated immediately, and then the field will be automatically cleared to'0'. |

**Table 20. Register Mapping and Definitions**

| Page | Offset | Access | Name | Description |
|---|---|---|---|---|
| 0 | 0 | RW | BMCR | Basic Mode Control Register. |
| 0 | 1 | RO | BMSR | Basic Mode Status Register. |
| 0 | 2 | RO | PHYID1 | PHY Identifier Register 1. |
| 0 | 3 | RO | PHYID2 | PHY Identifier Register 2. |
| 0 | 4 | RW | ANAR | Auto-Negotiation Advertising Register. |
| 0 | 5 | RO | ANLPAR | Auto-Negotiation Link Partner Ability Register. |
| 0 | 6 | RO | ANER | Auto-Negotiation Expansion Register. |
| 0 | 7 | RW | ANNPTR | Auto-Negotiation Next Page Transmit Register. |
| 0 | 8 | RO | ANNPRR | Auto-Negotiation Next Page Receive Register. |
| 0 | 9 | RW | GBCR | 1000Base-T Control Register. |
| 0 | 10 | RO | GBSR | 1000Base-T Status Register. |
| 0 | 11 ~ 12 | RO | RSVD | Reserved. |
| 0 | 13 | WO | MACR | MMD Access Control Register. |
| 0 | 14 | RW | MAADR | MMD Access Address Data Register. |
| 0 | 15 | RO | GBESR | 1000Base-T Extended Status Register. |
| 0xa42 | 16 ~ 17 | RO | RSVD | Reserved. |
| 0xa42 | 18 | RW | INER | Interrupt Enable Register. |
| 0xa42 | 19 ~ 23 | RO | RSVD | Reserved. |
| 0xa43 | 24 | RW | PHYCR1 | PHY Specific Control Register 1. |
| 0xa43 | 25 | RW | PHYCR2 | PHY Specific Control Register 2. |
| 0xa43 | 26 | RO | PHYSR | PHY Specific Status Register. |
| 0xa43 | 27 ~ 28 | RO | RSVD | Reserved. |
| 0xa43 | 29 | RO | INSR | Interrupt Status Register. |
| 0xa43 | 30 | RO | RSVD | Reserved. |
| 0xa43 | 31 | RW | PAGSR | Page Select Register. |
| 0xa46 | 20 | RW | PHYSCR | PHY Special Config Register. |
| 0xd04 | 16 | RW | LCR | LED Control Register. |

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| Page | Offset | Access | Name | Description |
|---|---|---|---|---|
| 0xd04 | 17 | RW | EEELCR | EEE LED Control Register. |
| 0xd08 | 21 | RW | MIICR | MII Control Register. |
| 0xd40 | 22 | RW | INTBCR | INTB Pin Control Register. |

*Note 1: To access the IEEE Standard Registers 0 to 15, the Page Select Register (PAGSR, Register 31) should be set as '0' or '0xa42'(default value).*
*Note 2: For example, to switch to Page 0xd04, set Register 31 Data = 0x0d04 (change to Page 0xd04). After LED setting, switch back to the PHY's IEEE Standard Registers, i.e. Page 0 or Page 0xa42 (Register 31 Data = 0 or 0xa42).*

## 8.2. MMD Register Mapping and Definitions

**Table 21. MMD Register Mapping and Definitions**

| Device | Offset | Access | Name | Description |
|---|---|---|---|---|
| 3 | 0 | RW | PC1R | PCS Control 1 Register. |
| 3 | 1 | RW | PS1R | PCS Status 1 Register. |
| 3 | 20 | RO | EEECR | EEE Capability Register. |
| 3 | 22 | RC | EEEWER | EEE Wake Error Register. |
| 7 | 60 | RW | EEEAR | EEE Advertisement Register. |
| 7 | 61 | RO | EEELPAR | EEE Link Partner Ability Register. |

## 8.3. Register Tables

### 8.3.1. BMCR (Basic Mode Control Register, Address 0x00)

**Table 22. BMCR (Basic Mode Control Register, Address 0x00)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 0.15 | Reset | RW, SC | 0 | Reset.<br>1: PHY reset<br>0: Normal operation<br>Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit 0.15 to 1).<br>This action may change the internal PHY state and the state of the physical link associated with the PHY. |
| 0.14 | Loopback | RW | 0 | Loopback Mode.<br>1: Enable PCS loopback mode<br>0: Disable PCS loopback mode<br>The loopback function enables RGMII transmit data to be routed to the RGMII receive data path. |

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| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 0.13 | Speed[0] | RW | 0 | Speed Select Bit 0.<br>In forced mode, i.e., when Auto-Negotiation is disabled, bits 0.6 and 0.13 determine device speed selection.<br>Speed[1] / Speed[0] / Speed Enabled:<br>1 / 1 / Reserved<br>1 / 0 / 1000Mbps<br>0 / 1 / 100Mbps<br>0 / 0 / 10Mbps |
| 0.12 | ANE | RW | 1 | Auto-Negotiation Enable.<br>1: Enable Auto-Negotiation<br>0: Disable Auto-Negotiation |
| 0.11 | PWD | RW | 0 | Power Down.<br>1: Power down (only Management Interface and logic are active; link is down)<br>0: Normal operation |
| 0.10 | Isolate | RW | 0 | Isolate.<br>1: RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211F(I)/RTL8211FD(I) ignores TXD[3:0], and TXCTL inputs, and presents a high impedance on RXC, RXCTL, RXD[3:0].<br>0: Normal operation |
| 0.9 | Restart_AN | RW, SC | 0 | Restart Auto-Negotiation.<br>1: Restart Auto-Negotiation<br>0: Normal operation |
| 0.8 | Duplex | RW | 0 | Duplex Mode.<br>1: Full Duplex operation<br>0: Half Duplex operation<br>This bit is valid only in force mode, i.e., NWay is disabled. |
| 0.7 | Collision Test | RW | 0 | Collision Test.<br>1: Collision test enabled<br>0: Normal operation |
| 0.6 | Speed[1] | RW | 1 | Speed Select Bit 1.<br>Refer to bit 0.13. |
| 0.5 | Uni-directional enable | RW | 0 | Uni-Directional Enable<br>1: Enable packet transmit without respect to linkok status<br>0: Packet transmit permitted when link is established |
| 0.4:0 | RSVD | RO | 00000 | Reserved. |

*Note 1: Changes to Registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD(0.11) transitions from power-down to normal operation.*

*Note 2: When the RTL8211F(I)/RTL8211FD(I) is switched from power down to normal operation, a software reset and restart auto-negotiation is performed, even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.*

*Note 3: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12 = 0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4, bit[8:5] and register 9, bit[9:8] take effect.*

*Note 4: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.*

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### 8.3.2. BMSR (Basic Mode Status Register, Address 0x01)

**Table 23. BMSR (Basic Mode Status Register, Address 0x01)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 1.15 | 100Base-T4 | RO | 0 | 100Base-T4 Capability.<br>The RTL8211F(I)/RTL8211FD(I) does not support 100Base-T4 mode. This bit should always be 0. |
| 1.14 | 100Base-TX (full) | RO | 1 | 100Base-TX Full Duplex Capability.<br>1: Device is able to perform 100Base-TX in full duplex mode<br>0: Device is not able to perform 100Base-TX in full duplex mode |
| 1.13 | 100Base-TX (half) | RO | 1 | 100Base-TX Half Duplex Capability.<br>1: Device is able to perform 100Base-TX in half duplex mode<br>0: Device is not able to perform 100Base-TX in half duplex mode |
| 1.12 | 10Base-T (full) | RO | 1 | 10Base-T Full Duplex Capability.<br>1: Device is able to perform 10Base-T in full duplex mode<br>0: Device is not able to perform 10Base-T in full duplex mode |
| 1.11 | 10Base-T (half) | RO | 1 | 10Base-T Half Duplex Capability.<br>1: Device is able to perform 10Base-T in half duplex mode<br>0: Device is not able to perform 10Base-T in half duplex mode |
| 1.10 | 100Base-T2 (full) | RO | 0 | 100Base-T2 Full Duplex Capability.<br>The RTL8211F(I)/RTL8211FD(I) does not support 100Base-T2 mode and this bit should always be 0. |
| 1.9 | 100Base-T2 (half) | RO | 0 | 100Base-T2 Half Duplex Capability.<br>The RTL8211F(I)/RTL8211FD(I) does not support 100Base-T2 mode. This bit should always be 0. |
| 1.8 | 1000Base-T Extended Status | RO | 1 | 1000Base-T Extended Status Register.<br>1: Device supports Extended Status Register 0x0F (15)<br>0: Device does not support Extended Status Register 0x0F<br>This register is read-only and is always set to 1. |
| 1.7 | Uni-directional ability | RO | 1 | Uni-directional ability.<br>1: PHY able to transmit from RGMII without linkok<br>0: PHY not able to transmit from RGMII without linkok |
| 1.6 | Preamble Suppression | RO | 0 | Preamble Suppression Capability.<br>The RTL8211F(I)/RTL8211FD(I) default will not accept MDC/MDIO transactions with preamble suppressed. |
| 1.5 | Auto-Negotiation Complete | RO | 0 | Auto-Negotiation Complete.<br>1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid<br>0: Auto-Negotiation process not complete |
| 1.4 | Remote Fault | RC, LH | 0 | Remote Fault.<br>1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner<br>0: No remote fault condition detected |
| 1.3 | Auto-Negotiation Ability | RO | 1 | Auto Configured Link.<br>1: Device is able to perform Auto-Negotiation<br>0: Device is not able to perform Auto-Negotiation |

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| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 1.2 | Link Status | RO | 0 | Link Status.<br>1: Linked<br>0: Not Linked<br>This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read Page 0xa43 Reg 26, bit[2] Link (Real Time). |
| 1.1 | Jabber Detect | RC, LH | 0 | Jabber Detect.<br>1: Jabber condition detected<br>0: No Jabber occurred |
| 1.0 | Extended Capability | RO | 1 | 1: Extended register capabilities, always 1 |

## 8.3.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

**Table 24. PHYID1 (PHY Identifier Register 1, Address 0x02)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 2.15:0 | OUI_MSB | RO | 0000000000011100 | Organizationally Unique Identifier Bit 3:18.<br>Always 0000000000011100. |

*Note: Realtek OUI number is 0x00E04Ch.*

## 8.3.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

**Table 25. PHYID2 (PHY Identifier Register 2, Address 0x03)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.15:10 | OUI_LSB | RO | 110010 | Organizationally Unique Identifier Bit 19:24.<br>Always 110010. |
| 3.9:4 | Model Number | RO | 010001 | Manufacturer's Model Number. |
| 3.3:0 | Revision Number | RO | 0110 | Revision Number. |

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### 8.3.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

**Table 26. ANAR (Auto-Negotiation Advertising Register, Address 0x04)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 4.15 | NextPage | RW | 0 | 1: Additional next pages exchange desired<br>0: No additional next pages exchange desired |
| 4.14 | RSVD | RO | 0 | Reserved. |
| 4.13 | Remote Fault | RW | 0 | 1: Set Remote Fault bit<br>0: No remote fault detected |
| 4.12 | RSVD | RO | 0 | Reserved. |
| 4.11 | Asymmetric PAUSE | RW | 0 | 1: Advertise support of asymmetric pause<br>0: No support of asymmetric pause |
| 4.10 | PAUSE | RW | 0 | 1: Advertise support of pause frames<br>0: No support of pause frames |
| 4.9 | 100Base-T4 | RO | 0 | 1: 100Base-T4 support<br>0: 100Base-T4 not supported |
| 4.8 | 100Base-TX (Full) | RW | 1 | 1: Advertise support of 100Base-TX full-duplex mode<br>0: Not advertised |
| 4.7 | 100Base-TX (Half) | RW | 1 | 1: Advertise support of 100Base-TX half-duplex mode<br>0: Not advertised |
| 4.6 | 10Base-T (Full) | RW | 1 | 1: Advertise support of 10Base-TX full-duplex mode<br>0: Not advertised |
| 4.5 | 10Base-T (Half) | RW | 1 | 1: Advertise support of 10Base-TX half-duplex mode<br>0: Not advertised |
| 4.4:0 | Selector Field | RO | 00001 | Indicates the RTL8211F(I)/RTL8211FD(I) supports IEEE 802.3 |

*Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down, i.e., software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.*
*Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.*

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## 8.3.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

**Table 27. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 5.15 | Next Page | RO | 0 | Next Page Indication.<br>Received Code Word Bit 15. |
| 5.14 | ACK | RO | 0 | Acknowledge.<br>Received Code Word Bit 14. |
| 5.13 | Remote Fault | RO | 0 | Remote Fault indicated by Link Partner.<br>Received Code Word Bit 13. |
| 5.12 | RSVD | RO | 0 | Reserved. |
| 5.11:5 | Technology Ability Field | RO | 00000000 | Received Code Word Bit 12:5. |
| 5.4:0 | Selector Field | RO | 00000 | Received Code Word Bit 4:0. |

*Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.3.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

**Table 28. ANER (Auto-Negotiation Expansion Register, Address 0x06)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 6.15:5 | RSVD | RO | 0x000 | Reserved. |
| 6.6 | RX NP location ability | RO | 1 | Received next page storage location ability.<br>1: Received next page storage location is specified by bit 6.5<br>0: Received next page storage location is not specified by bit 6.5 |
| 6.5 | RX NP location | RO | 1 | Received next page storage location.<br>1: Link partner next pages are stored in Register 8<br>0: Link partner next pages are stored in Register 5 |
| 6.4 | Parallel Detection Fault | RC, LH | 0 | 1: A fault has been detected via the Parallel Detection function<br>0: A fault has not been detected via the Parallel Detection function |
| 6.3 | Link Partner Next Page Able | RO | 0 | 1: Link Partner supports Next Page exchange<br>0: Link Partner does not support Next Page exchange |
| 6.2 | Local Next Page Able | RO | 1 | 1: Local Device is able to send Next Page<br>Always 1. |
| 6.1 | Page Received | RC, LH | 0 | 1: A New Page (new LCW) has been received<br>0: A New Page has not been received |
| 6.0 | Link Partner Auto-Negotiation capable | RO | 0 | 1: Link Partner supports Auto-Negotiation<br>0: Link Partner does not support Auto-Negotiation |

*Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

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## 8.3.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

**Table 29. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 7.15 | Next Page | RW | 0 | Next Page Indication.<br>0: No more next pages to send<br>1: More next pages to send<br>Transmit Code Word Bit 15. |
| 7.14 | RSVD | RO | 0 | Transmit Code Word Bit 14. |
| 7.13 | Message Page | RW | 1 | Message Page.<br>0: Unformatted Page<br>1: Message Page<br>Transmit Code Word Bit 13. |
| 7.12 | Acknowledge 2 | RW | 0 | Acknowledge2.<br>0: Local device has no ability to comply with the message received<br>1: Local device has the ability to comply with the message received<br>Transmit Code Word Bit 12. |
| 7.11 | Toggle | RO | 0 | Toggle Bit.<br>Transmit Code Word Bit 11. |
| 7.10:0 | Message/Unformatted Field | RW | 0x001 | Content of Message/Unformatted Page.<br>Transmit Code Word Bit 10:0. |

## 8.3.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

**Table 30. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 8.15 | Next Page | RO | 0 | Received Link Code Word Bit 15. |
| 8.14 | Acknowledge | RO | 0 | Received Link Code Word Bit 14. |
| 8.13 | Message Page | RO | 0 | Received Link Code Word Bit 13. |
| 8.12 | Acknowledge 2 | RO | 0 | Received Link Code Word Bit 12. |
| 8.11 | Toggle | RO | 0 | Received Link Code Word Bit 11. |
| 8.10:0 | Message/Unformatted Field | RO | 0x00 | Received Link Code Word Bit 10:0. |

*Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

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## 8.3.10. GBCR (1000Base-T Control Register, Address 0x09)

**Table 31. GBCR (1000Base-T Control Register, Address 0x09)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 9.15:13 | Test Mode | RW | 0 | Test Mode Select.<br>000: Normal Mode<br>001: Test Mode 1 – Transmit Jitter Test<br>010: Test Mode 2 – Transmit Jitter Test (MASTER mode)<br>011: Test Mode 3 – Transmit Jitter Test (SLAVE mode)<br>100: Test Mode 4 – Transmit Distortion Test<br>101, 110, 111: Reserved |
| 9.12 | MASTER/SLAVE Manual Configuration Enable | RW | 0 | Enable Manual Master/Slave Configuration.<br>1: Manual MASTER/SLAVE configuration<br>0: Automatic MASTER/SLAVE |
| 9.11 | MASTER/SLAVE Configuration Value | RW | 0 | Advertise Master/Slave Configuration Value.<br>1: Manual configure as MASTER<br>0: Manual configure as SLAVE |
| 9.10 | Port Type | RW | 0 | Advertise Device Type Preference.<br>1: Prefer multi-port device (MASTER)<br>0: Prefer single port device (SLAVE) |
| 9.9 | 1000Base-T Full Duplex | RW | 1 | Advertise 1000Base-T Full-Duplex Capability.<br>1: Advertise<br>0: Do not advertise |
| 9.8 | RSVD | RO | 0 | Reserved. |
| 9.7:0 | RSVD | RO | 0 | Reserved. |

*Note 1: Values set in register 9.12:9 have no effect unless Auto-Negotiation is restarted (Reg 0.9) or the link goes down.*
*Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12 = 0.*

## 8.3.11. GBSR (1000Base-T Status Register, Address 0x0A)

**Table 32. GBSR (1000Base-T Status Register, Address 0x0A)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 10.15 | MASTER/SLAVE Configuration Fault | RO, RC, LH | 0 | Master/Slave Manual Configuration Fault Detected.<br>1: MASTER/SLAVE configuration fault detected<br>0: No MASTER/SLAVE configuration fault detected |
| 10.14 | MASTER/SLAVE Configuration Resolution | RO | 0 | Master/Slave Configuration Result.<br>1: Local PHY configuration resolved to MASTER<br>0: Local PHY configuration resolved to SLAVE |
| 10.13 | Local Receiver Status | RO | 0 | Local Receiver Status.<br>1: Local Receiver OK<br>0: Local Receiver Not OK |
| 10.12 | Remote Receiver Status | RO | 0 | Remote Receiver Status.<br>1: Remote Receiver OK<br>0: Remote Receiver Not OK |
| 10.11 | Link Partner 1000Base-T Full Duplex Capability | RO | 0 | Link Partner 1000Base-T Full Duplex Capability.<br>1: Link Partner is capable of 1000Base-T full duplex<br>0: Link Partner is not capable of 1000Base-T full duplex |

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| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 10.10 | Link Partner 1000Base-T Half Duplex Capability | RO | 0 | Link Partner 1000Base-T Half Duplex Capability.<br>1: Link Partner is capable of 1000Base-T half duplex<br>0: Link Partner is not capable of 1000Base-T half duplex |
| 10.9:8 | RSVD | RO | 00 | Reserved. |
| 10.7:0 | Idle Error Count | RO, RC | 0x00 | MSB of Idle Error Counter.<br>The counter stops automatically when it reaches 0xff. |

*Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.*
*Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.3.12. MACR (MMD Access Control Register, Address 0x0D)

**Table 33. MACR (MMD Access Control Register, Address 0x0D)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 13.15:14 | Function | WO | 0 | 00: Address<br>01: Data with no post increment<br>10: Data with post increment on reads and writes<br>11: Data with post increment on writes only |
| 13.13:5 | RSVD | RO | 000000000 | Reserved. |
| 13.4:0 | DEVAD | WO | 0 | Device Address. |

*Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.*
*Note 2: If the MAADR accesses for address (Function = 00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.*
*Note 3: If the MAADR accesses for data (Function ≠ 00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.*

## 8.3.13. MAADR (MMD Access Address Data Register, Address 0x0E)

**Table 34. MAADR (MMD Access Address Data Register, Address 0x0E)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 14.15:0 | Address Data | RW | 0x0000 | 13.15:14 = 00<br>→ MMD DEVAD's address register<br>13.15:14 = 01, 10, or 11<br>→ MMD DEVAD's data register as indicated by the contents of its address register |

*Note: This register is used in conjunction with the MACR (Register 13; Table 33) to provide access to the MMD address space.*

## 8.3.14. GBESR (1000Base-T Extended Status Register, Address 0x0F)

**Table 35. GBESR (1000Base-T Extended Status Register, Address 0x0F)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 15.15 | 1000Base-X FD | RO | 0 | 0: Not 1000Base-X full duplex capable |
| 15.14 | 1000Base-X HD | RO | 0 | 0: Not 1000Base-X half duplex capable |
| 15.13 | 1000Base-T FD | RO | 1 | 1: 1000Base-T full duplex capable |
| 15.12 | 1000Base-T HD | RO | 0 | 1: 1000Base-T half duplex capable |
| 15.11:0 | RSVD | RO | 0x000 | Reserved. |

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## 8.3.15. INER (Interrupt Enable Register, Page 0xa42, Address 0x12)

**Table 36. INER (Interrupt Enable Register, Page 0xa42, Address 0x12)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 18.15:11 | RSVD | RW | 00000 | Reserved. |
| 18.10 | Jabber Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the jabber interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[10] always reflects the jabber interrupt behavior. |
| 18.9 | ALDPS State Change Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the ALDPS state change interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[9] always reflects the ALDPS state change interrupt behavior. |
| 18.8 | RSVD | RW | 0 | Reserved. |
| 18.7 | PME (Power Management Event of WOL) | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the PME interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[7] always reflects the PME interrupt behavior. |
| 18.6 | RSVD | RW | 0 | Reserved. |
| 18.5 | PHY Register Accessible Interrupt | RW | 1 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the PHY register access interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[5] always reflects the PHY register access interrupt behavior. |
| 18.4 | Link Status Change Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the link status change interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[4] always reflects the link change interrupt behavior. |
| 18.3 | Auto-Negotiation Completed Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the auto-negotiation completed interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[3] always reflects the auto-negotiation completed interrupt behavior. |
| 18.2 | Page Received Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the page received interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[2] always reflects the page received interrupt behavior. |
| 18.1 | RSVD | RW | 0 | Reserved. |
| 18.0 | Auto-Negotiation Error Interrupt | RW | 0 | 1: Interrupt Enable 0: Interrupt Disable<br>Setting this bit to 0 only disables the auto-negotiation error interrupt event in the INTB pin.<br>Page 0xa43, Reg29 Bit[0] always reflects the auto-negotiation error interrupt behavior. |

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## 8.3.16. PHYCR1 (PHY Specific Control Register 1, Page 0xa43, Address 0x18)

**Table 37. PHYCR1 (PHY Specific Control Register 1, Page 0xa43, Address 0x18)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 24.15:14 | RSVD | RO | 00 | Reserved. |
| 24.13 | PHYAD_0 Enable | RW | 1 | 1: A broadcast from MAC (A command with PHY address = 0) is valid. MDC/MDIO will respond to this command |
| 24.12 | ALDPS XTAL-OFF Enable | RW | 0 | 1: Enable XTAL off when in ALDPS mode (valid when Bit 24.2 = 1) |
| 24.11:10 | RSVD | RO | 00 | Reserved. |
| 24.9 | MDI Mode Manual Configuration Enable | RW | 0 | 1: Enable Manual Configuration of MDI mode |
| 24.8 | MDI Mode | RW | 1 | Set the MDI/MDIX mode.<br>1: MDI 0: MDIX<br>This bit will take effect only when Bit 24.9 = 1. |
| 24.7 | TX CRS Enable | RW | 0 | 1: Assert CRS on transmit<br>0: Never assert CRS on transmit |
| 24.6 | PHYAD Non-zero Detect | RW | 0 | 1: The RTL8211F(I)/RTL8211FD(I) with PHYAD[2:0] = 000 will latch the first non-zero PHY address as its own PHY address |
| 24.5 | RSVD | RO | 0 | Reserved. |
| 24.4 | Preamble Check Enable | RW | 1 | 1: Check preamble when receiving an MDC/MDIO command |
| 24.3 | Jabber Detection Enable | RW | 1 | 1: Enable Jabber Detection |
| 24.2 | ALDPS Enable | RW | 0 | 1: Enable Link Down Power Saving Mode |
| 24.1 | ALDPS PLL-OFF Enable | RW | 0 | 1: Enable PLL off when in ALDPS mode (valid when Bit 24.2 = 1) |
| 24.0 | RSVD | RO | 0 | Reserved. |

*Note: The method to disable auto-crossover and force MDI or MDIX mode is as follows:*
*Step 1: Set Bit 24.9 = 1 (Manual Configuration of MDI mode) and set Bit24.8 = 1 (MDI) or 0 (MDIX).*
*Step 2: Perform a PHY reset, i.e., set Page 0, Reg 0 bit[15] = 1.*

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### 8.3.17. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)

**Table 38. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 25.15:14 | RSVD | RO | 00 | Reserved. |
| 25.13:12 | CLKOUT SSC Capability | RW | 00 | CLKOUT SSC Capability Select.<br>00: Normal CLKOUT<br>11: CLKOUT with SSC capability<br>Others: Reserved |
| 25.11 | CLKOUT Frequency Select | RW | 1 | Frequency Select of the CLKOUT Pin Clock Output.<br>0: 25MHz<br>1: 125MHz |
| 25.10:8 | RSVD | RO | 000 | Reserved. |
| 25.7 | CLKOUT SSC Enable | RW | 0 | 1: Enable Spread-Spectrum Clocking (SSC) on CLKOUT output clock<br>*Note: Please refer to the RTL8211F_Series_EMI_Improvement_App_Note for detailed methods of enabling/disabling SSC.* |
| 25.6 | Center-tap Short Enable | RW | 1 | 1: The transformer center-tap is shorted<br>0: The transformer center-tap is not shorted<br>*Note: Please refer to the RTL8211F Series Xformer_CenterTap_Short_Patch_Application_Note for detailed information.* |
| 25.5 | PHY-mode EEE Enable | RW | 1 | 1: Enable EEE in PHY mode |
| 25.4 | RSVD | RO | 0 | Reserved. |
| 25.3 | SYSCLK SSC Enable | RW | 0 | 1: Enable Spread-Spectrum Clocking (SSC) on System Clock |
| 25.2 | RSVD | RO | 0 | Reserved. |
| 25.1 | RXC Enable | RW | 1 | 1: RXC Clock Output Enabled |
| 25.0 | CLKOUT Enable | RW | 1 | 1: CLKOUT Clock Output Enabled |

*Note 1: A PHY reset should be issued (set Page 0, Reg 0 bit[15] = 1) after setting these bits in PHYCR2 register.*
*Note 2: Refer to the RTL8211F_Series_EMI_Improvement_App_Note for detailed methods of enabling/disabling SSC.*

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## 8.3.18. PHYSR1 (PHY Specific Status Register 1, Page 0xa43, Address 0x1A)

**Table 39. PHYSR1 (PHY Specific Status Register 1, Page 0xa43, Address 0x1A)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 26.15 | RSVD | RO | 0 | Reserved. |
| 26.14 | ALDPS State | RO | 0 | Link Down Power Saving Mode.<br>1: Reflects local device entered Link Down Power Saving Mode, i.e., cable not plugged in (reflected after 3 sec)<br>0: With cable plugged in |
| 26.13 | MDI Plug | RO | 0 | MDI Status.<br>1: Plugged 0: Unplugged |
| 26.12 | NWay Enable | RO | 1 | Auto-Negotiation (NWay) Status.<br>1: Enable 0: Disable |
| 26.11 | Master Mode | RO | 0 | Device is in Master/Slave Mode.<br>1: Master mode 0: Slave mode |
| 26.10:9 | RSVD | RO | 00 | Reserved. |
| 26.8 | EEE capability | RO | 0 | 1: Both local and link-partner have EEE capability of current speed |
| 26.7 | Rxflow Enable | RO | 0 | Rx Flow Control.<br>1: Enable 0: Disable |
| 26.6 | Txflow Enable | RO | 0 | Tx Flow Control.<br>1: Enable 0: Disable |
| 26.5:4 | Speed | RO | 00 | Link Speed.<br>11: Reserved 10: 1000Mbps<br>01: 100Mbps 00: 10Mbps |
| 26.3 | Duplex | RO | 0 | Full/Half Duplex Mode.<br>1: Full duplex 0: Half duplex |
| 26.2 | Link (Real Time) | RO | 0 | Real Time Link Status.<br>1: Link OK 0: Link not OK |
| 26.1 | MDI Crossover Status | RO | 1 | MDI/MDI Crossover Status.<br>1: MDI 0: MDI Crossover |
| 26.0 | Jabber (Real Time) | RO | 0 | Real Time Jabber Indication.<br>1: Jabber Indication 0: No Jabber Indication |

*Note 1: Bit 26.11 valid only when in Giga mode.*
*Note 2: Bit 26.8 asserts at 10M speed when local device is EEE capable.*

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## 8.3.19. INSR (Interrupt Status Register, Page 0xa43, Address 0x1D)

**Table 40. INSR (Interrupt Status Register, Page 0xa43, Address 0x1D)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 29.15:11 | RSVD | RO, RC | 00000 | Reserved. |
| 29.10 | Jabber | RO, RC | 0 | 1: Jabber detected 0: No jabber detected |
| 29.9 | ALDPS State Change | RO, RC | 0 | 1: ALDPS state changed<br>0: ALDPS state not changed |
| 29.8 | RSVD | RO, RC | 0 | Reserved. |
| 29.7 | PME (Power Management Event of WOL) | RO, RC | 0 | 1: WOL event occurred<br>0: WOL event did not occur |

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 29.6 | RSVD | RO, RC | 0 | Reserved. |
| 29.5 | PHY Register Accessible | RO, RC | 0 | 1: Can access PHY Register through MDC/MDIO<br>0: Cannot access PHY Register through MDC/MDIO |
| 29.4 | Link Status Change | RO, RC | 0 | 1: Link status changed 0: Link status not changed |
| 29.3 | Auto-Negotiation Completed | RO, RC | 0 | 1: Auto-Negotiation completed<br>0: Auto-Negotiation not completed |
| 29.2 | Page Received | RO, RC | 0 | 1: Page (a new LCW) received<br>0: Page not received |
| 29.1 | RSVD | RO, RC | 0 | Reserved. |
| 29.0 | Auto-Negotiation Error | RO, RC | 0 | 1: Auto-Negotiation Error 0: No Auto-Negotiation Error |

## 8.3.20. PAGSR (Page Select Register, Page 0xa43, Address 0x1F)

**Table 41. PAGSR (Page Select Register, Page 0xa43, Address 0x1F)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 31.15:12 | RSVD | RO | 0 | Reserved. |
| 31.11:0 | PageSel | RW | 0xa42 | Page Select (in HEX).<br>0xa42: Page 0xa42 (default page) |

## 8.3.21. PHYCR3 (PHY Specific Control Register 3, Page 0xa44, Address 0x11)

**Table 42. PHYCR3 (PHY Specific Control Register 3, Page 0xa44, Address 0x11)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 17.15:11 | RSVD | RO | 0 | Reserved. |
| 17.10:5 | RSVD | RW | 100001 | Reserved. |
| 17.4 | Thr_retry_spdn | RW | 1 | Retry Times before Speed down:<br>1: 3 times<br>0: 7 times |
| 17.3 | En_retry_spdn | RW | 1 | 1: Enable retry speed down |
| 17.2 | En_two-Pair_spdn | RW | 1 | 1: Enable two-pair speed down |
| 17.1:0 | RSVD | RO | 0 | Reserved. |

## 8.3.22. PHYSCR (PHY Special Config Register, Page 0xa46, Address 0x14)

**Table 43. PHYSCR (PHY Specific Config Register, Page 0xa46, Address 0x14)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 20.15:2 | RSVD | RO | 0 | Reserved. |
| 20.1 | PHY Special Config Done | RW | 0 | 1: Write 1 to indicate the special PHY parameter configuration has been done |
| 20.0 | RSVD | RO | 0 | Reserved. |

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## 8.3.23. PHYSR2 (PHY Specific Status Register 2, Page 0xa4b, Address 0x10)

**Table 44. PHYSR2 (PHY Specific Status Register 2, Page 0xa4b, Address 0x10)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 16.15:13 | RSVD | RO | 0 | Reserved. |
| 16.12 | Linkok_retry_spdn | RO,LH,SC | 0 | 1: Linkok due to retry speed down |
| 16.11 | Linkok_ 2Pair_spdn | RO,LH,SC | 0 | 1: Linkok due to two-pair speed down |
| 16.10:0 | RSVD | RO | 0 | Reserved. |

## 8.3.24. LCR (LED Control Register, Page 0xd04, Address 0x10)

**Table 45. LCR (LED Control Register, Page 0xd04, Address 0x10)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 16.15 | LED_MODE | RW | 0 | 0: LED Mode A is selected<br>1: LED Mode B is selected |
| 16.14 | LED2_ACT | RW | 1 | LED2 Active (Transmitting or Receiving) Indication. |
| 16.13 | LED2_LINK_1000 | RW | 1 | LED2 Link Indication: 1000Mbps |
| 16.12 | RSVD | RO | 0 | Reserved. |
| 16.11 | LED2_LINK_100 | RW | 0 | LED2 Link Indication: 100Mbps |
| 16.10 | LED2_LINK_10 | RW | 0 | LED2 Link Indication: 10Mbps |
| 16.9 | LED1_ACT | RW | 1 | LED1 Active (Transmitting or Receiving) Indication. |
| 16.8 | LED1_LINK_1000 | RW | 0 | LED1 Link Indication: 1000Mbps |
| 16.7 | RSVD | RO | 0 | Reserved. |
| 16.6 | LED1_LINK_100 | RW | 1 | LED1 Link Indication: 100Mbps |
| 16.5 | LED1_LINK_10 | RW | 0 | LED1 Link Indication: 10Mbps |
| 16.4 | LED0_ACT | RW | 1 | LED0 Active (Transmitting or Receiving) Indication. |
| 16.3 | LED0_LINK_1000 | RW | 0 | LED0 Link Indication: 1000Mbps |
| 16.2 | RSVD | RO | 0 | Reserved. |
| 16.1 | LED0_LINK_100 | RW | 0 | LED0 Link Indication: 100Mbps |
| 16.0 | LED0_LINK_10 | RW | 1 | LED0 Link Indication: 10Mbps |

## 8.3.25. EEELCR (EEE LED Control Register, Page 0xd04, Address 0x11)

**Table 46. EEELCR (EEE LED Control Register, Page 0xd04, Address 0x11)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 17.15:4 | RSVD | RO | 0 | Reserved. |
| 17.3 | LED2 EEE Enable | RW | 1 | 1: Enable EEE LED indication of LED2 |
| 17.2 | LED1 EEE Enable | RW | 1 | 1: Enable EEE LED indication of LED1 |
| 17.1 | LED0 EEE Enable | RW | 1 | 1: Enable EEE LED indication of LED0 |
| 17.0 | RSVD | RO | 0 | Reserved. |

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## 8.3.26. MIICR1 (MII Control Register 1, Page 0xd08, Address 0x11)

**Table 47. MIICR1 (MII Control Register 1, Page 0xd08, Address 0x11)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 17.15:9 | RSVD | RO | 0 | Reserved. |
| 17.8 | TXDLY Enable | RW | 0 | 1:Enable RGMII TXDLY |
| 17.7:4 | RSVD | RO | 0 | Reserved. |
| 17.3:0 | RSVD | RO | 1001 | Reserved. |

## 8.3.27. MIICR2 (MII Control Register 2, Page 0xd08, Address 0x15)

**Table 48. MIICR2 (MII Control Register 2, Page 0xd08, Address 0x15)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 21.15:7 | RSVD | RO | 0 | Reserved. |
| 21.6 | RGMII In-band CRS Enable | RW | 0 | 1: Enable in-band CRS Status in RGMII Rx flow |
| 21.5:4 | RSVD | RO | 0 | Reserved. |
| 21.3 | RXDLY Enable | RW | 1 | 1:Enable RGMII RXDLY |
| 21.2:0 | RSVD | RO | 0 | Reserved. |

## 8.3.28. INTBCR (INTB Pin Control Register, Page 0xd40, Address 0x16)

**Table 49. INTBCR (INTB Pin Control Register, Page 0xd40, Address 0x16)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 22.15:6 | RSVD | RO | 0 | Reserved. |
| 22.5 | INTB/PMEB Selection | RW | 0 | Pin 31 of the RTL8211F(D)(I) functions as:<br>1: PMEB<br>0: INTB |
| 22.4:0 | RSVD | RO | 0 | Reserved. |

## 8.3.29. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

**Table 50. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.0.15:11 | RSVD | RW | 0 | Reserved. |
| 3.0.10 | Clock Stop Enable | RW | 0 | 1: PHY stops RXC when receiving LPI<br>0: RXC not stoppable |
| 3.0.9:0 | RSVD | RW | 0 | Reserved. |

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## 8.3.30. PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

**Table 51. PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.1.15:12 | RSVD | RO | 0 | Reserved. |
| 3.1.11 | TX LPI Received | RO, LH | 0 | 1: TX PCS has received LPI<br>0: LPI not received |
| 3.1.10 | RX LPI Received | RO, LH | 0 | 1: RX PCS has received LPI<br>0: LPI not received |
| 3.19 | TX LPI Indication | RO | 0 | 1: TX PCS is currently receiving LPI<br>0: TX PCS is not currently receiving LPI |
| 3.1.8 | RX LPI Indication | RO | 0 | 1: RX PCS is currently receiving LPI<br>0: RX PCS is not currently receiving LPI |
| 3.1.7 | RSVD | RO | 0 | Reserved. |
| 3.1.6 | Clock Stop Capable | RO | 1 | 1: MAC stops TXC in LPI<br>0: TXC not stoppable |
| 3.1.5:0 | RSVD | RO | 0 | Reserved. |

## 8.3.31. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

**Table 52. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.20.15:3 | RSVD | RO | 0 | Reserved. |
| 3.20.2 | 1000Base-T EEE | RO | 1 | 1: EEE is supported for 1000Base-T EEE<br>0: EEE is not supported for 1000Base-T EEE |
| 3.20.1 | 100Base-TX EEE | RO | 1 | 1: EEE is supported for 100Base-TX EEE<br>0: EEE is not supported for 100Base-TX EEE |
| 3.20.0 | RSVD | RO | 0 | Reserved. |

## 8.3.32. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

**Table 53. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.22.15:0 | EEE Wake Error Counter | RC | 0 | Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. |

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### 8.3.33. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

**Table 54. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 7.60.15:3 | RSVD | RW | 0 | Reserved. |
| 7.60.2 | 1000Base-T EEE | RW | 1 | Advertise 1000Base-T EEE Capability.<br>1: Advertise 0: Do not advertise |
| 7.60.1 | 100Base-TX EEE | RW | 1 | Advertise 100Base-TX EEE Capability.<br>1: Advertise 0: Do not advertise |
| 7.60.0 | RSVD | RW | 0 | Reserved. |

### 8.3.34. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

**Table 55. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 7.61.15:3 | RSVD | RO | 0 | Reserved. |
| 7.61.2 | LP 1000Base-T EEE | RO | 0 | 1: Link Partner is capable of 1000Base-T EEE<br>0: Link Partner is not capable of 1000Base-T EEE |
| 7.61.1 | LP 100Base-TX EEE | RO | 0 | 1: Link Partner is capable of 100Base-TX EEE<br>0: Link Partner is not capable of 100Base-TX EEE |
| 7.61.0 | RSVD | RO | 0 | Reserved. |

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# 9. Regulators and Power Sequence

## *9.1. Switching Regulator (RTL8211F(I) Only)*

The RTL8211F(I) incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The switching regulator 1.0V output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

Use an X5R/X7R low-ESR ceramic capacitor as the output capacitor for switching regulator stability.

*Note: Refer to the RTL8211F Series Layout Guide for detailed description.*

## *9.2. Low-Dropout Regulator (RTL8211FD(I) Only)*

The RTL8211FD(I) incorporates a linear Low-Dropout Regulator (LDO) that features high power supply ripple rejection and low output noise. The built-in LDO means a power inductor is not required for the RTL8211FD(I); only an output capacitor is required between the 1.0V output and the analog ground for phase compensation, which saves cost and PCB real estate.

Use an X5R/X7R low-ESR ceramic capacitor, with capacitance of at least 0.1uF, to enhance the stability of output voltage. The bypass capacitors should be placed as close as possible to power pins (AVDD10 and DVDD10) for adequate filtering.

The regulator 1.0V output pin (LDO_OUT) should be connected only to DVDD10 and AVDD10 pins (do not provide this power source to other devices).

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## 9.3. Power Sequence

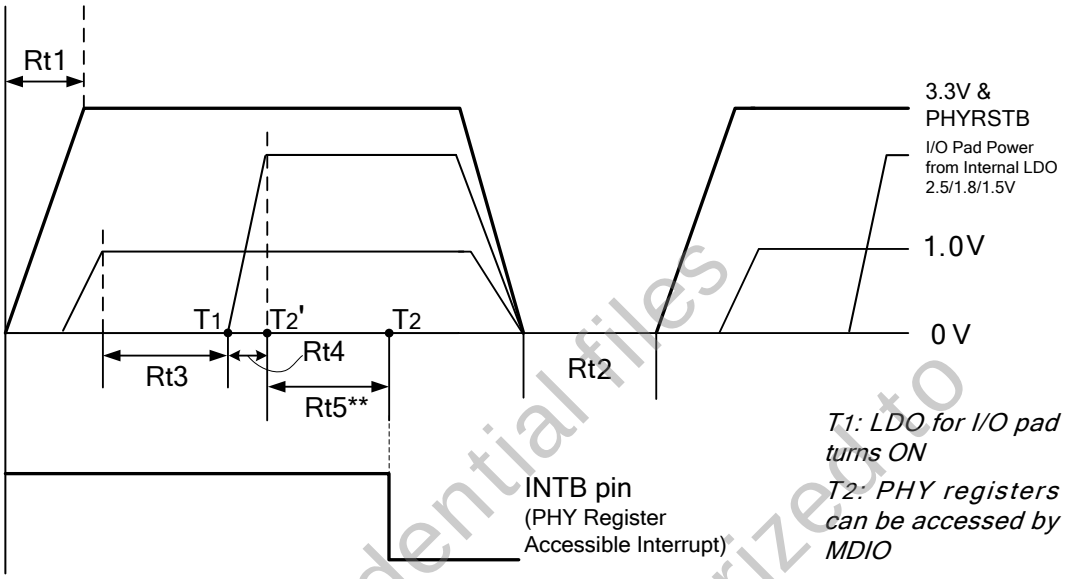


**Figure 10. Power Sequence (I/O Pad Power Sourced from Internal LDO)**

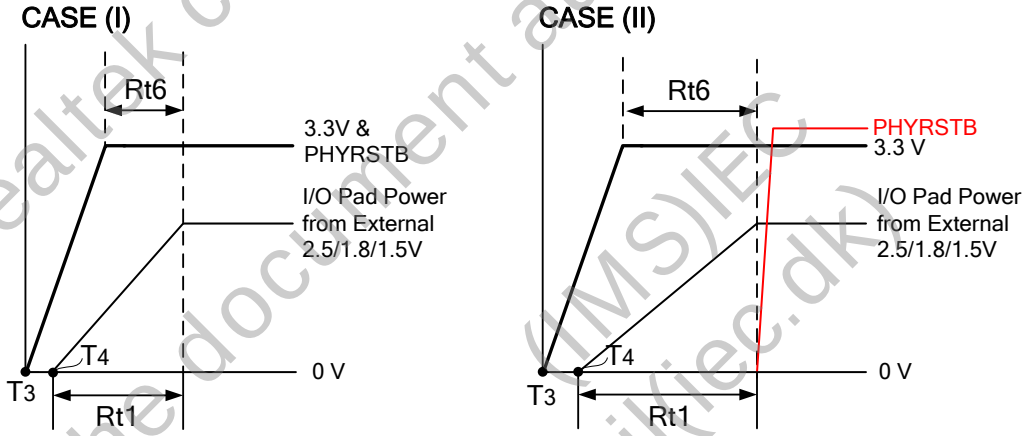


**Figure 11. Power Sequence (I/O Pad Power Sourced Externally)**

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**Table 56. Power Sequence Parameters**

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Rt1 | 3.3V Rise Time.<br>External I/O Pad Power Rise Time. | 0.5* | - | 100 | ms |
| Rt2 | 3.3V Off Time. | 100 | - | - | ms |
| Rt3 | Core Logic Ready Time. | - | - | 72 | ms |
| Rt4 | LDO Ready Time. | - | - | 1.5 | ms |
| Rt5** | Reserved for Specific Parameter Configuration. | 100 | - | - | ms |
| Rt6 | External I/O Pad Power Ready Time after 3.3V Ready. | 0 | - | 5 | ms |

*Note 1: The RTL8211F(I)/RTL8211FD(I) does not support fast 3.3V rising. The 3.3V rise time should be controlled over 0.5ms.*
** A 3.3V rise time between 0.1ms to 0.5ms is conditionally permitted only if the system 3.3V power budget is sufficient to ensure that 3.3V Overcurrent Protection (OCP) will NOT be triggered during the power-on procedure. If the rise time is less than 0.1ms, it will induce a peak voltage in DVDD33 which may cause permanent damage to the regulator.*
*Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.0V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 100ms.*
*Note 3: When using an external oscillator or clock source, on stopping the clock source the RTL8211F(I)/RTL8211FD(I) must also be powered off.*
*Note 4: The RTL8211F(I)/RTL8211FD(I) use the integrated LDO to generate the 2.5V, 1.8V/1.5V voltages for the I/O pad, the I/O pad voltage can be selected by using the CONFIG pins CFG_LDO[1:0]. Moreover, external power source for the I/O pad is also supported, please refer to the setting of CFG_EXT and CFG_LDO[1:0] pins (section 7.8 Hardware Configuration, page 14).*
*Note 5: We recommend users to reserve the maximum value time of Rt3/Rt4.*
*Note 6: When using an external power source for the I/O pad, the power should rise simultaneously or slightly later than 3.3V power, i.e. $T_4$ □ $T_3$ in Figure 11.*
*Furthermore, there are two kinds of timing specifications to supply the external power, respectively:*
*Ready time of the external power should be within 5ms after 3.3V is ready. See CASE(I) in Figure 11, page 49.*
*PHYRSTB should be kept low until the external power is ready. See CASE(II) in Figure 11, page 49. Note that for this case, there is no constraint on the 'max' value of Rt6.*
*Violation of these timing constraints may lead to errors.*
*Note 7: Rt5 is a reserved window for some PHY special parameter configurations with 100ms duration. The parameters, if needed, can be provided by Realtek. At the point of $T_2$, i.e. the end of this configuration window, all the PHY registers can be accessed through MDIO*
*** Currently there is no special configuration needed for the RTL8211F(D)(I); the Rt5 can be skipped by setting Page 0xa46, Reg. 20, bit[1] = 1 (PHY Special Config Done) at the point of $T_2$. The 'PHY Register Accessible Interrupt' will then trigger accordingly, which indicates the PHY registers can be accessed by MDIO.*

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# 10. Characteristics

## 10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 57. Absolute Maximum Ratings**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VDD33, AVDD33 | Supply Voltage 3.3V. | -0.3 | 3.7 | V |
| AVDD10, DVDD10 | Supply Voltage 1.0V. | -0.3 | 1.2 | V |
| 2.5V RGMII/GMII | Supply Voltage 2.5V. | -0.2 | 2.8 | V |
| 1.8V RGMII | Supply Voltage 1.8V. | -0.2 | 2.3 | V |
| 1.5V RGMII | Supply Voltage 1.5V. | -0.2 | 2.0 | V |
| 3.3V DCinput<br>3.3V DCoutput | Input Voltage.<br>Output Voltage. | -0.3 | 3.6 | V |
| 1.0V DCinput<br>1.0V DCoutput | Input Voltage.<br>Output Voltage. | -0.3 | 1.2 | V |
| NA | Storage Temperature. | -55 | +125 | °C |

*Note: Refer to the most updated schematic circuit for correct configuration.*

## 10.2. Recommended Operating Conditions

**Table 58. Recommended Operating Conditions**

| Description | Pins | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage VDD. | DVDD33, AVDD33 | 2.97 | 3.3 | 3.63 | V |
| | AVDD10, DVDD10 | 0.95 | 1.0 | 1.05 | V |
| | 2.5V RGMII/GMII | 2.25 | 2.5 | 2.75 | V |
| | 1.8V RGMII | 1.62 | 1.8 | 1.98 | V |
| | 1.5V RGMII | 1.5 | 1.56 | 1.62 | V |
| Ambient Operating Temperature $T_A$ (RTL8211F/RTL8211FD). | - | 0 | - | 70 | °C |
| Ambient Operating Temperature $T_A$ (RTL8211FI/RTL8211FDI). | - | -40 | - | 85 | °C |
| Maximum Junction Temperature. | - | - | - | 125 | °C |

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## 10.3. Crystal Requirements

**Table 59. Crystal Requirements**

| Symbol | Description/Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| $F_{ref}$ | Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type. | - | 25 | - | MHz |
| $F_{ref}$ Tolerance | Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type.<br>$T_a$ = 0°C ~ 70°C. (RTL8211F/RTL8211FD)<br>$T_a$ = -40°C ~ 85°C. (RTL8211FI/RTL8211FDI) | -50 | - | +50 | ppm |
| $F_{ref}$ Duty Cycle | Reference Clock Input Duty Cycle. | 40 | - | 60 | % |
| ESR | Equivalent Series Resistance. | - | - | 50 | Ω |
| DL | Drive Level. | - | - | 0.5 | mW |
| $V_{ih}$_CKXTAL | Crystal Output High Level | 1.4 | - | - | V |
| $V_{il}$_CKXTAL | Crystal Output Low Level | - | - | 0.4 | V |

*Note 1: $F_{ref}$ Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.*

## 10.4. Oscillator/External Clock Requirements

**Table 60. Oscillator/External Clock Requirements**

| Parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Frequency | - | - | 25 | - | MHz |
| Frequency Tolerance (RTL8211F/RTL8211FD) | Ta = 0°C ~ 70°C | -50 | - | 50 | ppm |
| Frequency Tolerance (RTL8211FI/RTL8211FDI) | Ta = -40°C ~ 85°C | -50 | - | 50 | ppm |
| Duty Cycle | - | 40 | - | 60 | % |
| Broadband Peak-to-Peak Jitter [1, 2] | - | - | - | 200 | ps |
| $V_{ih}$ | - | 1.4 | - | - | V |
| $V_{il}$ | - | - | - | 0.4 | V |
| Rise Time (10% ~ 90%) | - | 1 | - | 10 | ns |
| Fall Time (10% ~ 90%) | - | 1 | - | 10 | ns |
| Operating Temperature Range (RTL8211F/RTL8211FD) | - | 0 | - | 70 | °C |
| Operating Temperature Range (RTL8211FI/RTL8211FDI) | - | -40 | - | 85 | °C |

*Note 1: 10kHz to 20Mhz RMS<3ps.*
*Note 2: Broadband RMS < 9ps.*
*Note 3: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.*

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## 10.5. DC Characteristics

**Table 61. DC Characteristics**

| Symbol | Parameter | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| VDD33, AVDD33 | 3.3V Supply Voltage | - | 2.97 | 3.3 | 3.63 | V |
| 1. MDIO (Table 4, page 8), MDC<br>2. RGMII I/O (Table 3, page 8) | 2.5V RGMII Supply Voltage | - | 2.25 | 2.5 | 2.75 | V |
| 1. MDIO (Table 4, page 8), MDC<br>2. RGMII I/O (Table 3, page 8) | 1.8V RGMII Supply Voltage | - | 1.62V | 1.8V | 1.98V | V |
| 1. MDIO (Table 4, page 8), MDC<br>2. RGMII I/O (Table 3, page 8) | 1.5V RGMII Supply Voltage | - | 1.5V | 1.56V | 1.62V | V |
| DVDD10, AVDD10 | 1.0V Supply Voltage | - | 0.95 | 1.0 | 1.05 | V |
| $V_{oh}$ (3.3V) | Minimum High Level Output Voltage | - | 2.4 | - | VDD33 + 0.3 | V |
| $V_{oh}$ (2.5V) | Minimum High Level Output Voltage | - | 2.0 | - | VDD25 + 0.3 | V |
| $V_{oh}$ (1.8V) | Minimum High Level Output Voltage | - | 0.9*VDD18 | - | VDD18 + 0.3 | V |
| $V_{oh}$ (1.5V) | Minimum High Level Output Voltage | - | 0.9*VDD15 | - | VDD15 + 0.3 | V |
| $V_{ol}$ (3.3V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| $V_{ol}$ (2.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.4 | V |
| $V_{ol}$ (1.8V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD18 | V |
| $V_{ol}$ (1.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD15 | V |
| $V_{ih}$ (3.3V) | Minimum High Level Input Voltage | - | 2.0 | - | - | V |
| $V_{il}$ (3.3V) | Maximum Low Level Input Voltage | - | - | - | 0.8 | V |
| Vih (2.5V) | Minimum High Level Input Voltage | - | 1.7 | - | - | V |
| Vil (2.5V) | Maximum Low Level Input Voltage | - | - | - | 0.7 | V |
| Vih (1.8V) | Minimum High Level Input Voltage | - | 1.2 | - | - | V |
| Vil (1.8V) | Maximum Low Level Input Voltage | - | - | - | 0.5 | V |
| Vih (1.5V) | Minimum High Level Input Voltage | - | 1.0 | - | - | V |
| Vil (1.5V) | Maximum Low Level Input Voltage | - | - | - | 0.3 | V |
| $I_{in}$ | Input Current | Vin = VDD33 or GND | 0 | - | 0.5 | µA |

*Note: Pins not mentioned above remain at 3.3V.*

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# 10.6. AC Characteristics

## 10.6.1. MDC/MDIO Timing

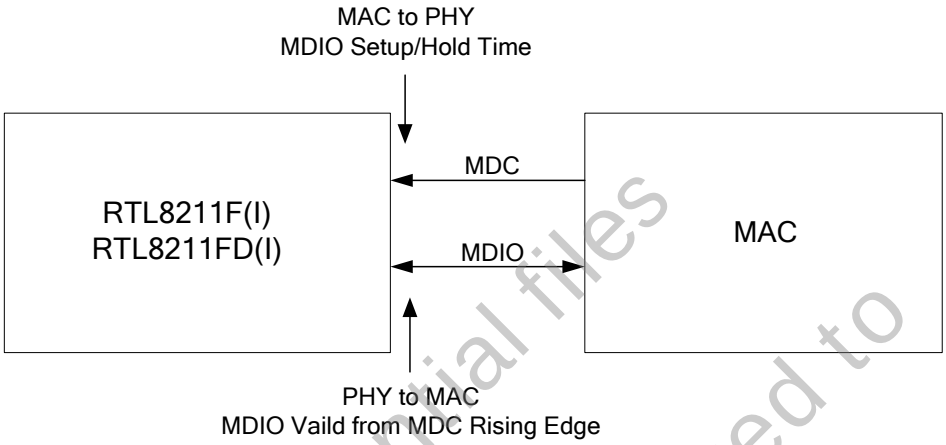


**Figure 12. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions**

**MDC/MDIO Timing – Management Port**

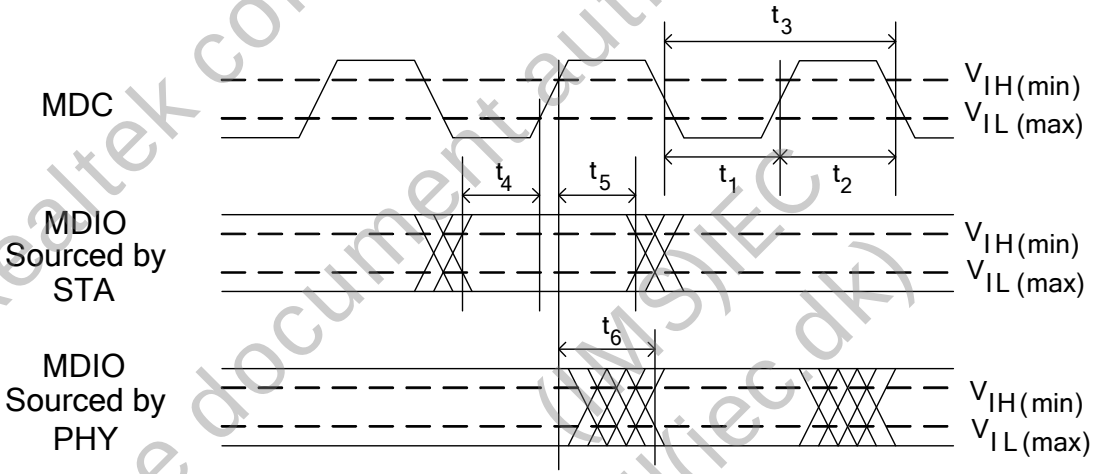


**Figure 13. MDC/MDIO Management Timing Parameters**

**Table 62. MDC/MDIO Management Timing Parameters**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_1$ | MDC High Pulse Width. | 32 | - | ns |
| $t_2$ | MDC Low Pulse Width. | 32 | - | ns |
| $t_3$ | MDC Period. | 80 | - | ns |
| $t_4$ | MDIO Setup to MDC Rising Edge. | 10 | - | ns |
| $t_5$ | MDIO Hold Time from MDC Rising Edge. | 10 | - | ns |
| $t_6$ | MDIO Valid from MDC Rising Edge. | 0 | 60 | ns |

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## 10.6.2. RGMII Timing Modes

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation.

Figure 14 shows the effect of adding an additional delay to TXC via the PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.

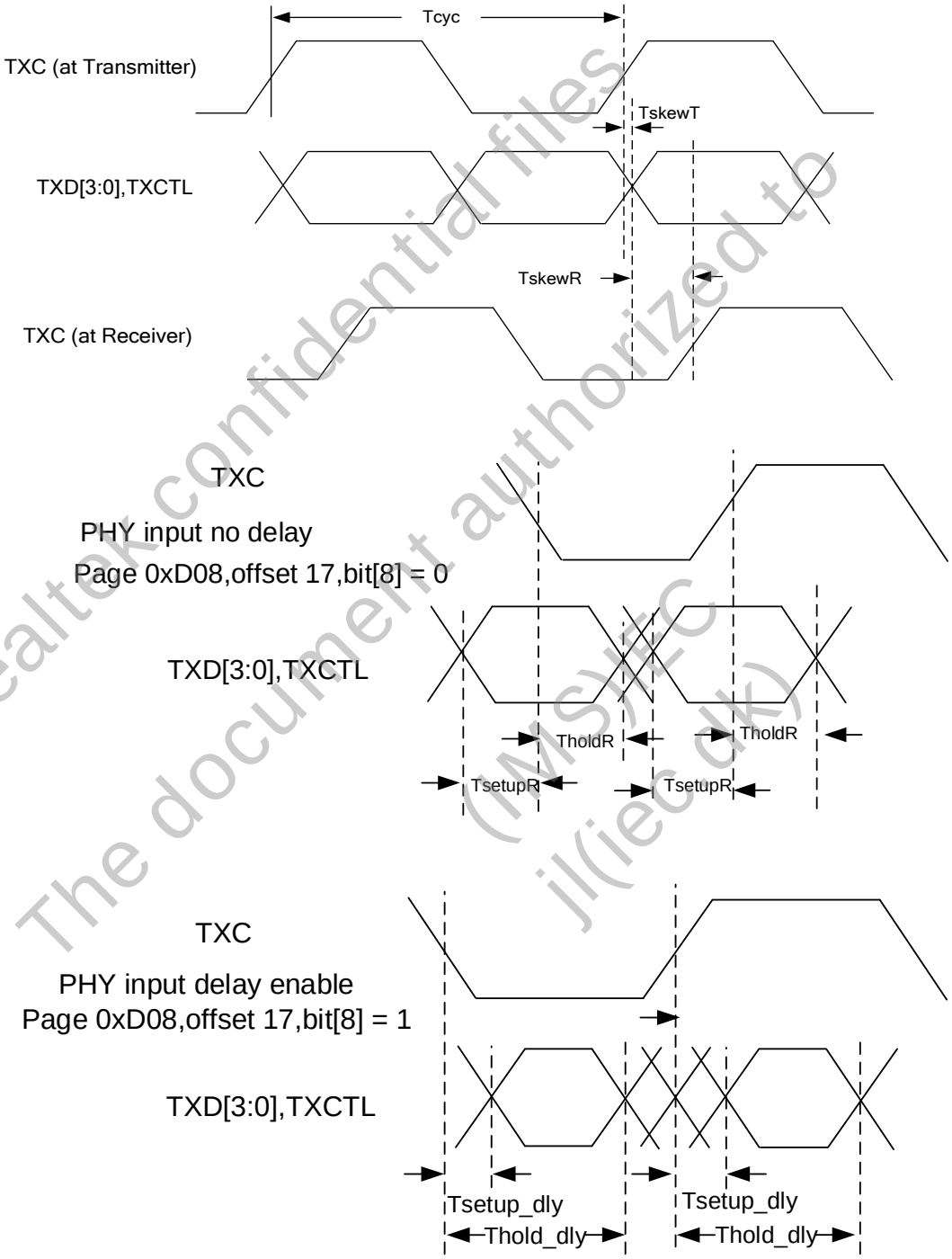


**Figure 14. RGMII Timing Modes (For TXC)**

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Figure 15 shows the effect of adding an additional delay to RXC via the PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.

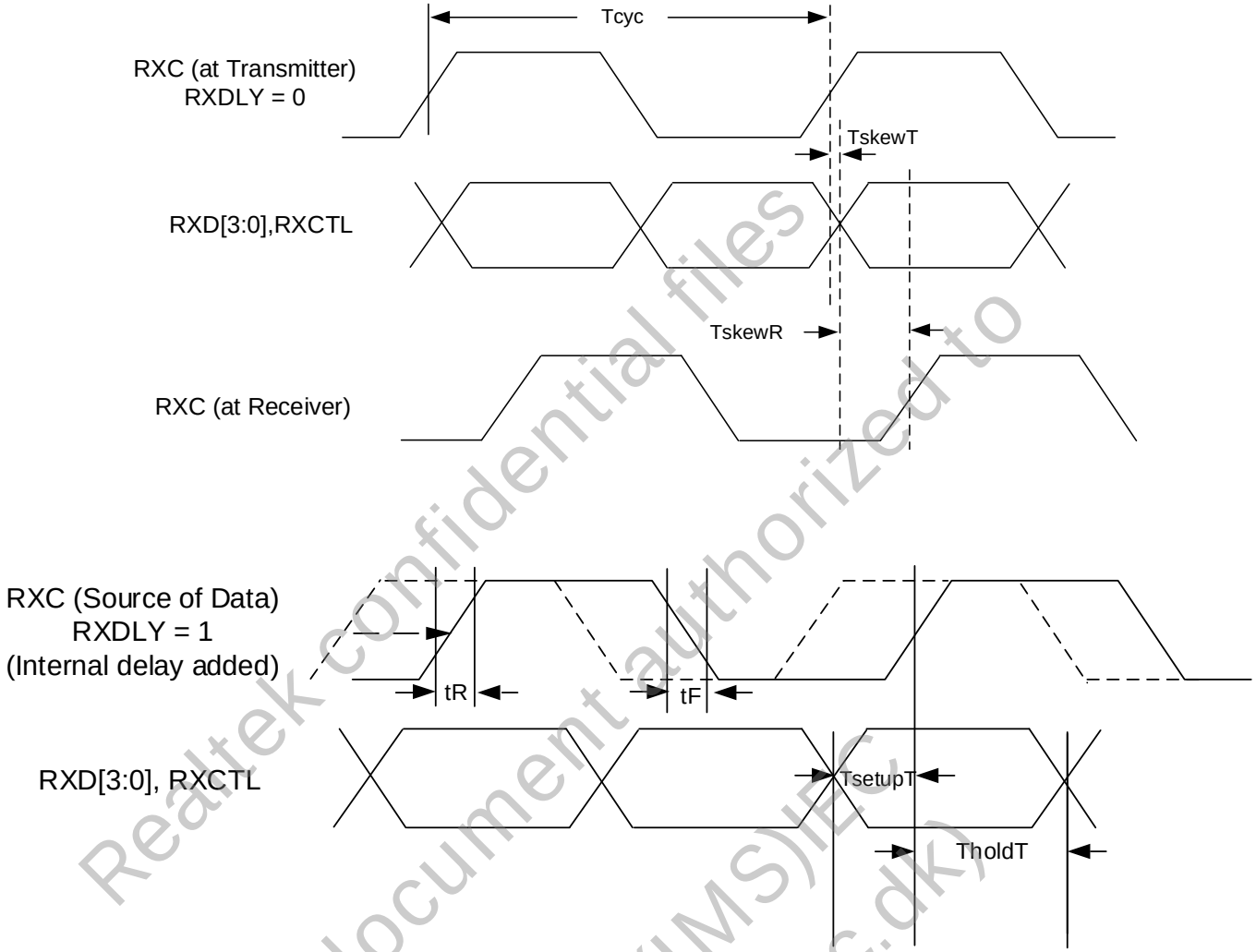


**Figure 15. RGMII Timing Modes (For RXC)**

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**Table 63. RGMII Timing Parameters**

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tcyc * | Clock Cycle Duration (1000Mbps). | 7.2 | 8 | 8.8 | ns |
| | Clock Cycle Duration (100Mbps). | 36 | 40 | 44 | ns |
| | Clock Cycle Duration (10Mbps). | 360 | 400 | 440 | ns |
| Duty_G | Duty Cycle for 1000. | 45 | 50 | 55 | % |
| Duty_T | Duty Cycle for 10/100. | 40 | 50 | 60 | % |
| tR | TXC/RXC Rise Time (20% ~ 80%). | - | - | 0.75 | ns |
| tF | TXC/RXC Fall Time (20% ~ 80%). | - | - | 0.75 | ns |
| TsetupT | Data to Clock Output Setup Time at transmitter (with delay integrated at transmitter). | 1.2 | 2 | - | ns |
| TholdT | Clock to Data Output Hold Time at transmitter (with delay integrated at transmitter). | 1.2 | 2 | - | ns |
| TsetupR | Data to Clock Input Setup Time at receiver (with delay integrated at transmitter). | 1.0 | 2 | - | ns |
| TholdR | Clock to Data Input Hold Time at receiver (with delay integrated at transmitter). | 1.0 | 2 | - | ns |
| Tsetup_dly | Data to Clock Input Setup Time (with delay integrated at receiver). | -0.6 | - | - | ns |
| Thold_dly | Clock to Data Input Hold Time (with delay integrated at receiver). | 3 | - | - | ns |
| TskewT ** | Data to Clock Output Skew Time at transmitter (without delay integrated). | -0.5 | 0 | 0.5 | ns |
| TskewR ** | Data to Clock Input Skew Time at receiver (with PCB delay integrated). This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. | 1 | 1.8 | 2.6 | ns |

**Note: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.*

***Note: For 10/100Mbps, the max value of Skew Time is unspecified.*

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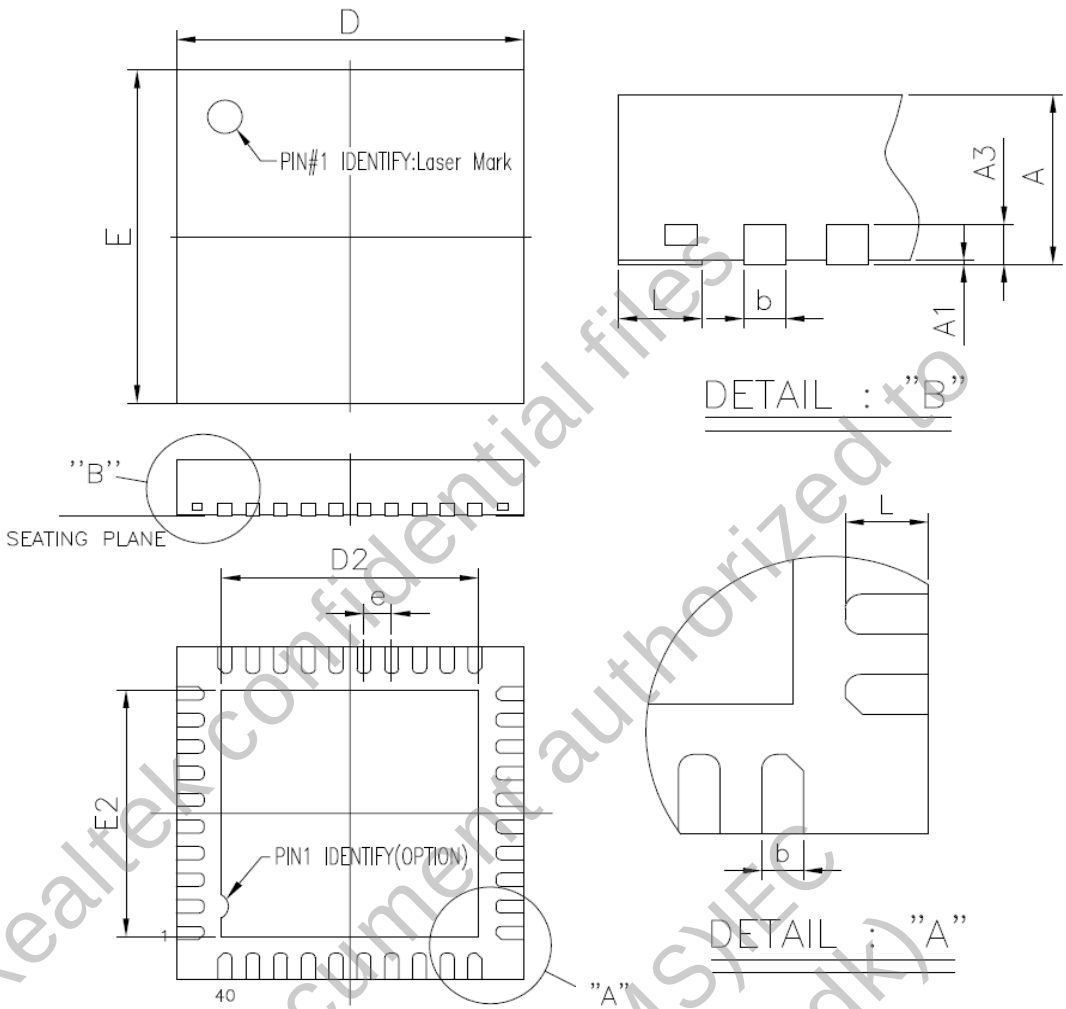
# 11. Mechanical Dimensions




## 11.1. Mechanical Dimensions Notes

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom. | Max | Min | Nom. | Max |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| $A_1$ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| $A_3$ | 0.20REF | | | 0.008REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 5.00 BSC | | | 0.197 BSC | | |
| D2/E2 | 3.45 | 3.60 | 3.75 | 0.136 | 0.142 | 0.148 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

*Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).*
*Note 2: REFERENCE DOCUMENT: JEDEC MO-220.*

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# 12. Ordering Information

**Table 64. Ordering Information**

| Part Number | Package | Status |
|---|---|---|
| RTL8211F-CG | 40-Pin QFN with 'Green' Package (Switching Regulator model) | MP |
| RTL8211FD-CG | 40-Pin QFN with 'Green' Package (LDO model) | MP |
| RTL8211FI-CG | 40-Pin QFN with 'Green' Package (Switching Regulator model) Industrial grade. | MP |
| RTL8211FDI-CG | 40-Pin QFN with 'Green' Package (LDO model). Industrial grade. | MP |

*Note: See page 6 for package identification.*

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