RTL8211F(D)(I)(-VD)
RTL8211FS(I)(-VS)
RTL8211FG(I)(-VS)

INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

LAYOUT GUIDE

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This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

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- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
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- Always disconnect the microcontroller from the prototyping board when it is being worked on

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REVISION HISTORY

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1.1	2014/04/12	Corrected minor typing errors.
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1. Introduction

The Realtek RTL8211F(D)(I)(-VD)/RTL8211FS(I)(-VS)/RTL8211FG(I)(-VS)-CG* are highly integrated Ethernet transceivers that comply with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. They provide all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5 UTP cable.

The RTL8211F series use state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211F to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) or Gigabit Media Independent Interface (GMII) for 1000Base-T, 10Base-T, and 100Base-TX. The RTL8211F series supports various signaling voltages for RGMII/GMII, including 3.3, 2.5, 1.8, and 1.5V* (only 3.3 and 2.5V are supported in GMII mode).

Note: For simplicity, if not individually specified the RTL8211F(D)(I)(-VD)/ RTL8211FS(I)(-VS)/RTL8211FG(I)(-VS)-CG will be called the 'RTL8211F series' or 'RTL8211F PHY' in the rest of this document.

Note: Do not support 1.5V RGMII for RTL8211F(D)(I)-VD, please refer the datasheet to find detail information.

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2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8211F series. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment

(2) Reduce the degree of EMI/EMC and their influence on the RTL8211F series.

(3) Simplify the task of routing signal traces

In order to achieve maximum performance using the RTL8211F series, good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

2.1. Placement

- The RTL8211F PHY must be placed as close as possible to the MAC (less than 15cm)
- The resistor connected to the RSET pin should be placed close to the RTL8211F PHY (less than 800 mils), and as far away as possible from signal traces (e.g. REG_OUT, MDIP0/MDIN0, MDIP1/MDIN1, etc.) and clock signals (50 mils min.)
- For good EMI performance, the PHY device must be placed as close as possible to the MAC (less than 15cm). If the MAC is placed on the top layer, then the PHY should be put on the bottom layer to avoid heat sink coupling

Note: For RTL8211F(D)(I)-VD, the distance between MAC must be less than 30cm.

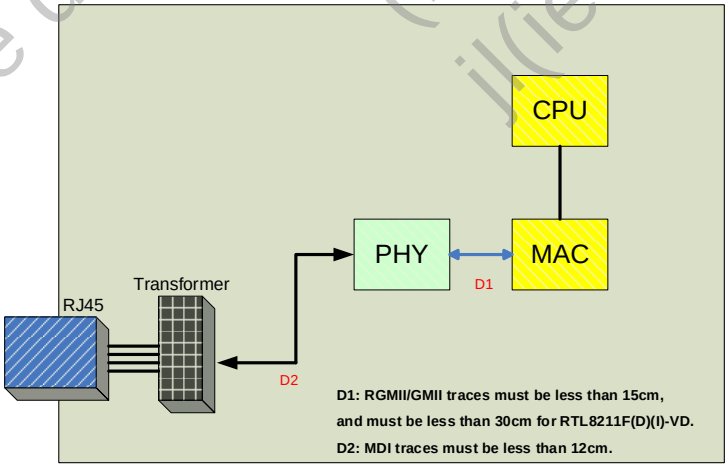

Figure 1. RGMII and MDI Placement

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2.2. Magnetics

- The 10/100/1000M magnetics should be placed as close as possible to the RJ-45 connector. The MDI traces must be less than 12cm.
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other.

2.3. Crystal/OSC

- Following the 3W rule, the Crystal should be placed at least three times its own width from I/O ports, important or high frequency signal traces (Tx, Rx, and power), and magnetics.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.

2.4. Ferrite Beads and De-Coupling Capacitors

Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors must be placed close to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

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3. Signal and Trace Routing

Noise, ringing, and data lines must be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

3.1. RX Clock (RXC)

- Clock signal traces should be kept as short and wide as possible.
- Route the receive reference clock traces adjacent to an unbroken ground or power plane. Minimize vias and layer changes.

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3.2. MDI Signals

- Traces routed from the RTL8211F series to the 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8211F PHY and magnetics is achievable only when there is no interference.
  It is also very important to keep all four differential pair signal traces (MDIP0/MDIN0, MDIP1/MDIN1, etc.) at matching lengths (within 800mil). MDI impedance is 100ohm in differential mode.
  The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is 8mil, then D1 can be 8mil wide (Figure 2).

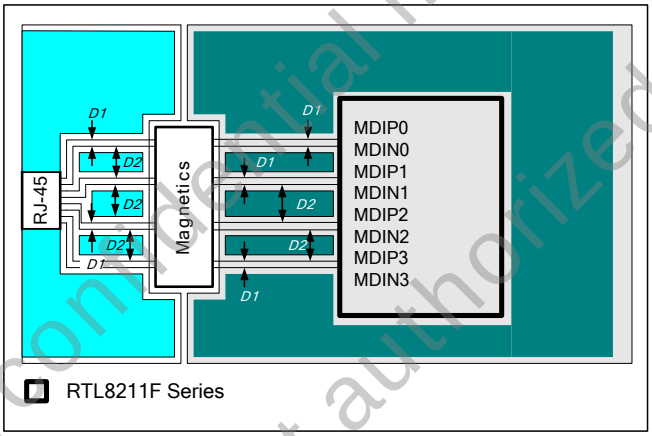

Figure 2. MDI Signals

- We suggest that there should be more than 30mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2 in Figure 2). In addition, Ground Plane shielding can be used to separate all four signal pairs.
  A good layout should avoid the following situations:
  --Intersection of any two pairs of signal traces.
  --Intersection of the two signal traces of the same differential pair.

- To minimize impedance mismatch, we recommend not using vias on the four differential pairs.

- The length difference of the signals in a pair(ex: MDIP0 and MDIN0) should not exceed 5 mils.

- Signals crossing a plane split (see Figure 3) may cause unpredictable return path currents and would likely result in signal quality failure, as well as induce EMI problems.

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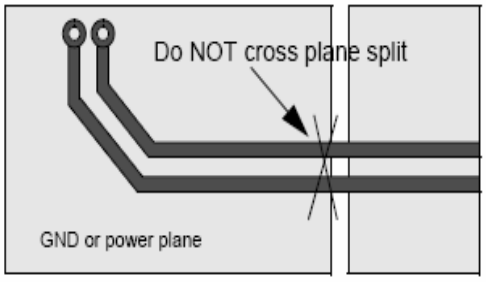

Figure 3. Signal Trace

3.3. GMII(MII)/RGMII Signals

- To ensure correct RGMII function, the input loading and length of the PCB trace should strictly comply with that defined in RGMII standard ver. 1.3, that is, maximum 1ns delay transmission line (about 15cm) with a 5pF input loading. For the best performance of RGMII with 1.5V signaling, the total trace loading (5pF input loading included) should be within 15pF.
- Ninety-degree trace turns must be avoided. We recommend that the traces turn at 45° angles as shown in Figure 4. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

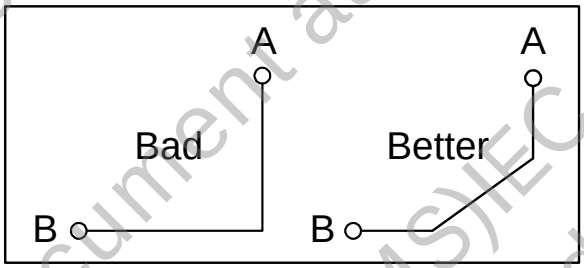

Figure 4. Signal Trace Angles

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- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high-speed signal traces must be as short as possible (less than 15cm or less than 30cm for RTL8211F(D)(I)-VD). It is better to have a ground plane under these traces. Using a GND plane to surround them is necessary.
- RXC and TXC are high-speed (125MHz) signals; keep a 20 mils space between clock and data signals.
- Match each GMII(MII)/RGMII Tx and Rx (RXC/RXD/RXCTL/RXDV) group trace length to within 100 mils.
- Route the GMII(MII)/RGMII traces at 50ohm impedance, and route through an inner layer to reduce radiation.

- Keep all GMII(MII)/RGMII traces as short as possible (less than 15cm or less than 30cm for RTL8211F(D)(I)-VD).
- All GMII(MII)/RGMII traces must be referenced to an unbroken ground plane.
- Place R1/C1 close to the RTL8211F PHY (must be less than 500 mils).

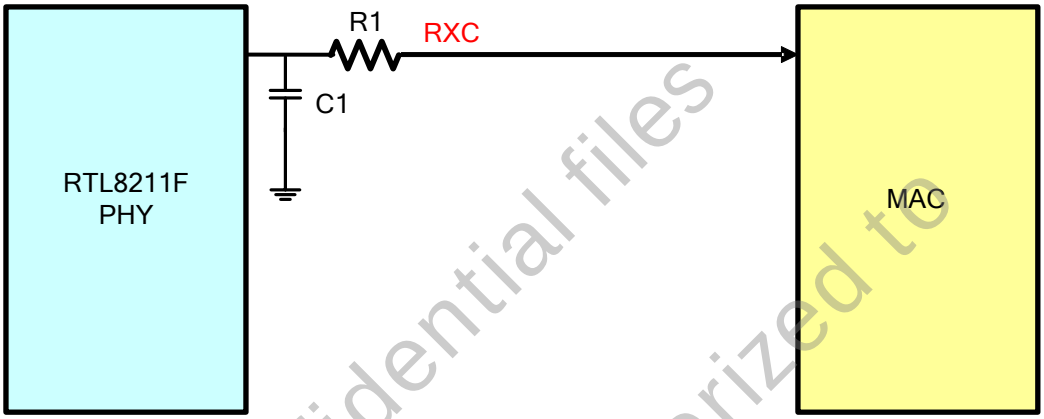

Figure 5. R1/C1 Placement

- Some return current paths, e.g., clock buffer and clock trace, can couple with the heat sink via parasitic capacitance, then radiate to air from the heat sink. To avoid this, RGMII traces must be routed away from the heat sink.

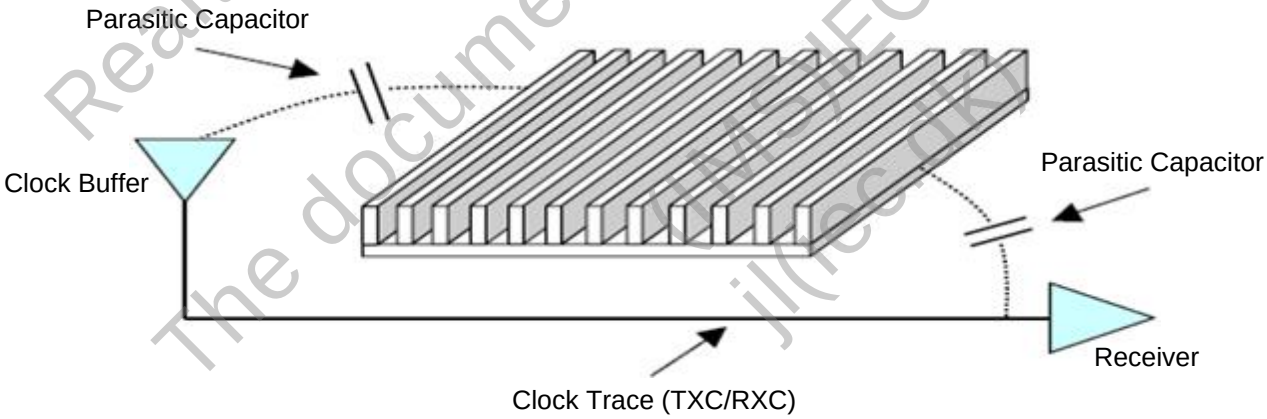

Figure 6. Clock and Heat Sink

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- Route the GMII(MII)/RGMII traces away from I/O traces to avoid crosstalk (>20 mils).

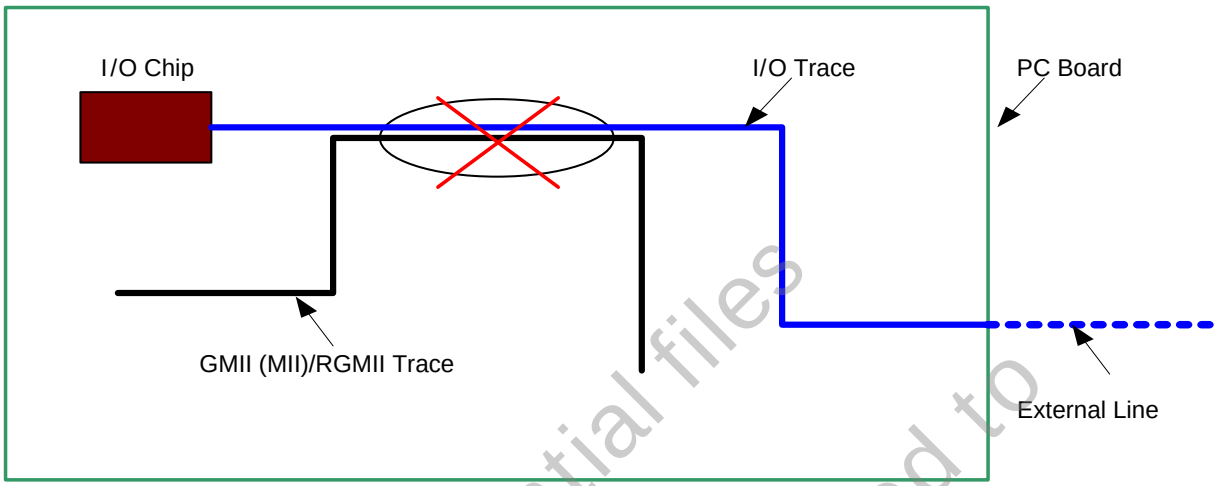

Figure 7. Clock and I/O Trace

3.3.1. Reserve 1.5/1.8/2.5V Power for RGMII Use (RTL8211F(D)(I)(-VD))

The RTL8211F(D)(I)(-VD) uses pin 28 for 1.5/1.8/2.5V RGMII from the external power source (related mode configuration should be selected).

Note: Do not support 1.5V RGMII for RTL8211F(D)(I)-VD.

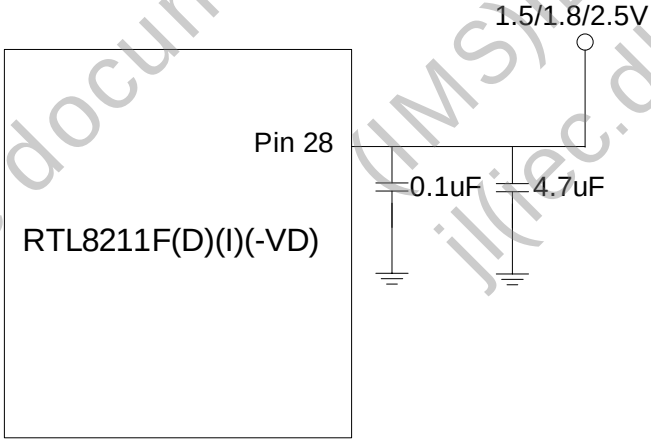

Figure 8. Reserve 1.5/1.8/2.5V Power for RGMII Use

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3.3.2. Reserved 1.5/1.8/2.5V Power for GMII/RGMII Use (RTL8211FG(I)(-VS))

The RTL8211FG(I)(-VS) uses pin 43 for 2.5V GMII or 1.5/1.8/2.5V RGMII from the external power source (related mode configuration should be selected).

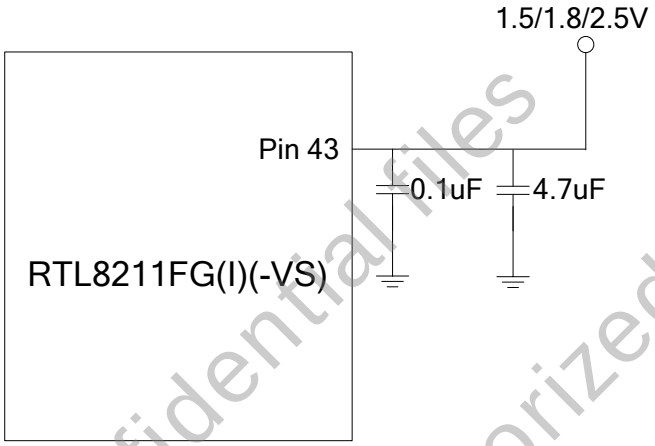

Figure 9. Reserved 1.5/1.8/2.5V Power for GMII/RGMII Use

3.4. SerDes Signals

As the SerDes transmits over 1.25/2.5/5GHz differential signal pairs, the PCB layout needs some attention in order to meet layout guidelines. This section lists some important guidelines for layout of the SerDes.

- Differential pair impedance is 100Ω±10%, and single-ended impedance is 60Ω±6%
- All micro-strip traces of a differential pair should be 5 mil-wide with 7 mil-wide air-gap spacing between the traces of the pair in a 4-layer PCB (see Figure 10) or 7 mil-wide with 5 mil-wide air-gap spacing between the traces of the pair in a 2-layer PCB (see Figure 11)
- Spacing to all non-SerDes signals should be at least 30 mil in order to avoid harmful coupling issues

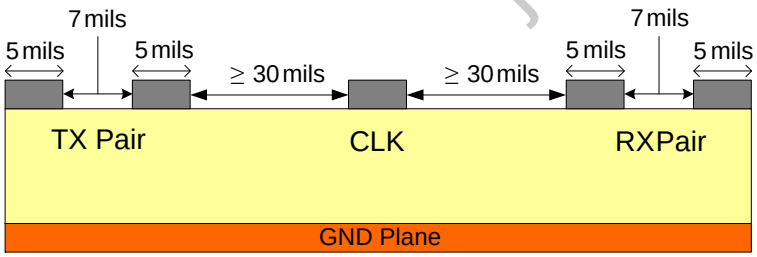

Figure 10. Trace Width and Spacing Recommendation for Microstrip in a 4-Layer PCB

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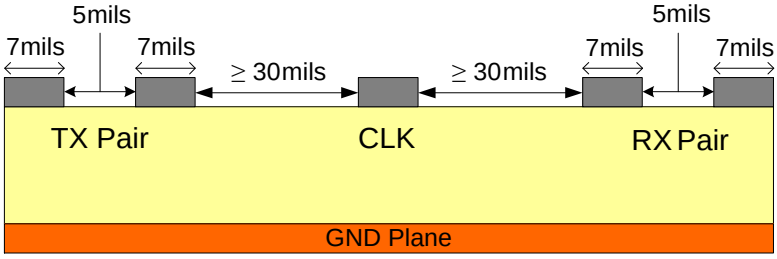

Figure 11. Trace Width and Spacing Recommendation for Microstrip in a 2-Layer PCB

- Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric. See Figure 12 for an illustration of diagonal routing

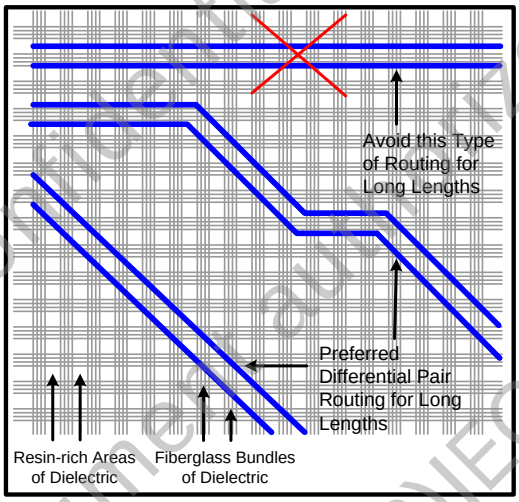

Figure 12. Long Trace Layout for SerDes

- Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible (see Figure 13)

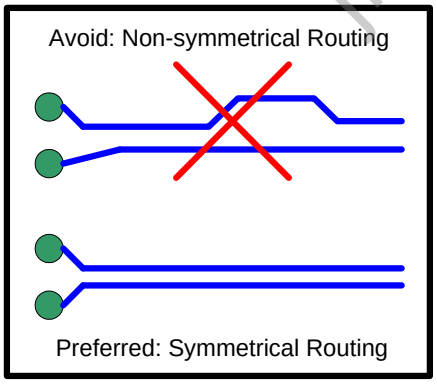

Figure 13. Symmetrical Routing

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- Keep differential pair routing lengths to less than 10 inches.
- Match the length of both sets of the differential pairs, allowing no more than a 5 mil delta between the lengths of the two signals
- Length matching should occur on a segment-by-segment basis vs. across the total distance of the overall route
- Differential pairs should have a continuous reference plane, and avoid vias
- Size 0402 AC coupling capacitors are strongly encouraged, as the smaller the package size, the less ESL
- Place AC coupling capacitors near output pins of differential pairs
- Locate capacitors for coupled traces at the same location along the differential traces and near output pins of differential pairs (see Figure 14)

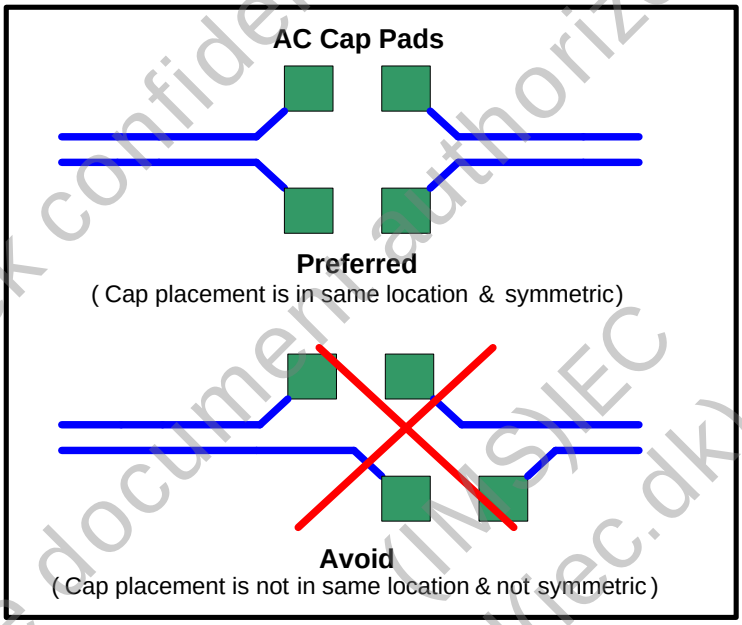

Figure 14. Symmetrical Routing Into AC Capacitors

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3.5. Power Signals

The power supply into the RTL8211F series digital power pins can be improved with de-coupling capacitors. The power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8211F PHY need to be de-coupled with a capacitor. The de-coupling capacitors must be placed close to the RTL8211F PHY (<200 mils), and the traces should be kept short.

4. PCB Stack-Up

4.1. Overview

PCB stack-up is a major factor affecting the EMC performance of a product. A good stack-up effectively reduces radiation from the loops on the PCB (differential-mode emissions), as well as from the cables connected to the board (common-mode emissions). Conversely, a poor stack-up may increase the radiation from both of these items considerably.

When using a multi-layer board, there are four main objectives to achieve:

1. Power and Ground planes should be coupled as closely as possible.

2. A signal layer should always be adjacent to a plane, and should be tightly coupled (close) to the adjacent plane.

3. High-speed signals (e.g. GMII/RGMII traces) must be routed on buried layers between planes so that the planes can act as shields and contain any radiation from the high-speed traces.

4. Multiple ground planes are very advantageous, since they will lower the ground (reference plane) impedance of the board and reduce the common-mode radiation.

The following are some recommendations to improve EMI performance.

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4.2. Four-Layer Stack-Up (Motherboard Application)

MDI and GMII/RGMII signals are routed on layer 4 and reference layer 3 (GND plane)

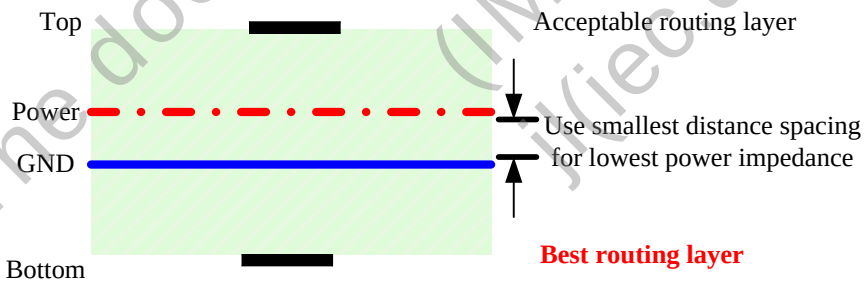

Figure 15. Four-Layer Stack-Up

4.3. Six-Layer Stack-Up (Notebook Application)

GMII/RGMII signals are routed on layer 4 (IN2) and reference layer 5 (GND plane)

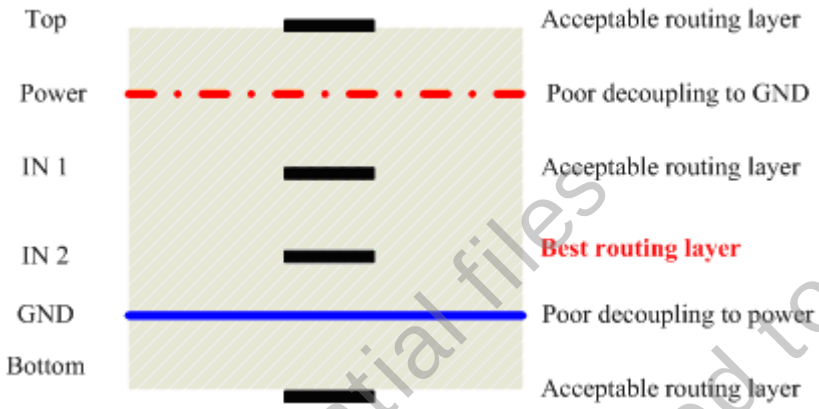

Figure 16. Six-Layer Stack-Up (A)

GMII/RGMII signals are routed on layer 4 (IN1) and reference layer 3 (GND plane)

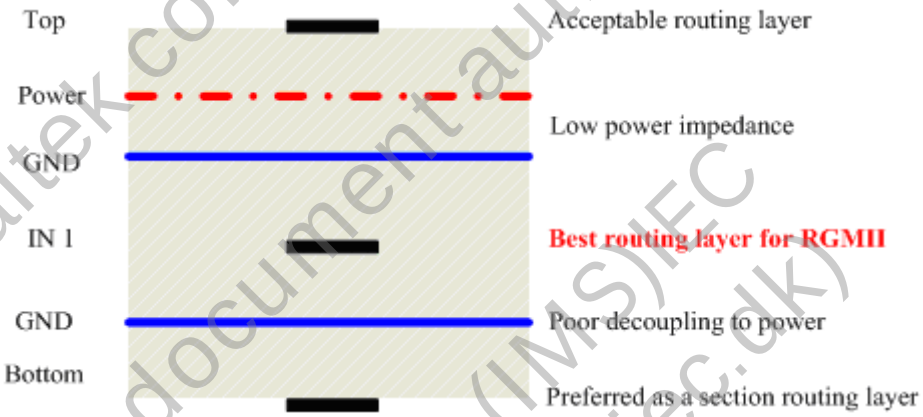

Figure 17. Six-Layer Stack-Up (B)

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GMII/RGMII signals are routed on layer 3 (IN1) and reference layer 2 (GND plane)

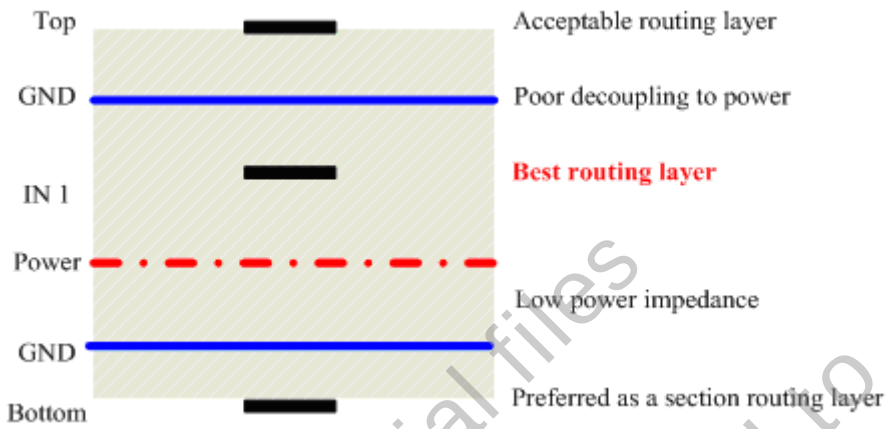

Figure 18. Six-Layer Stack-Up (C)

4.4. Eight-Layer Stack-Up (Notebook Application)

GMII/RGMII signals are routed on layer 3 (IN1) or layer 6 (IN3), and reference layer 2 (GND plane) or layer 7 (GND plane)

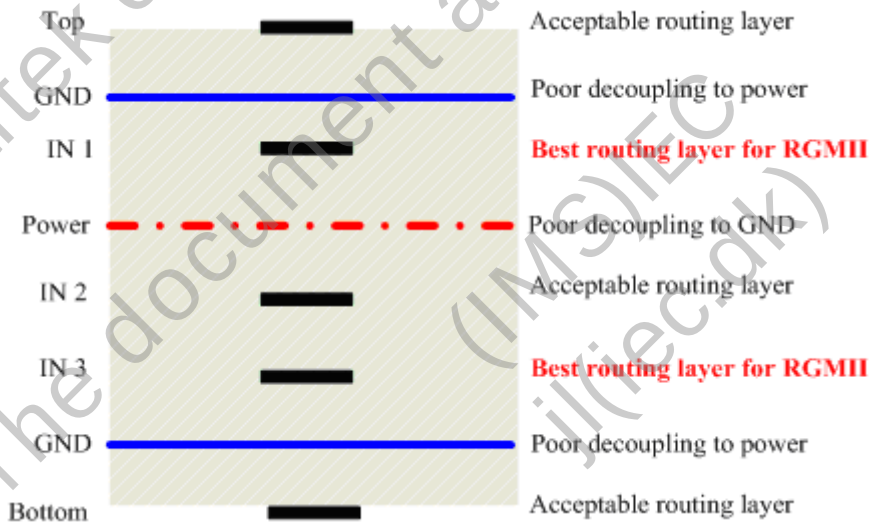

Figure 19. Eight-Layer Stack-Up

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5. Ground Plane Layout

Isolated separation between Analog and Digital Ground domains is not recommended, as bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

The RTL8211F series has only a single ground plane for analog power (AVDD33 and AVDD10(09)) and digital power (DVDD33, DVDD10(09), DVDD_RG). In the center of the IC, there is an Exposed Pad (E-PAD) ground. The PCB layout requires 9 vias to connect the E-PAD to the lower layer ground plane (see Figure 20).

Note:

RTL8211F(D)(I)-VD: AVDD09, DVDD09

RTL8211F(D)(I), RTL8211FS(I)(-VS), RTL8211FG(I)(-VS): AVDD10, DVDD10

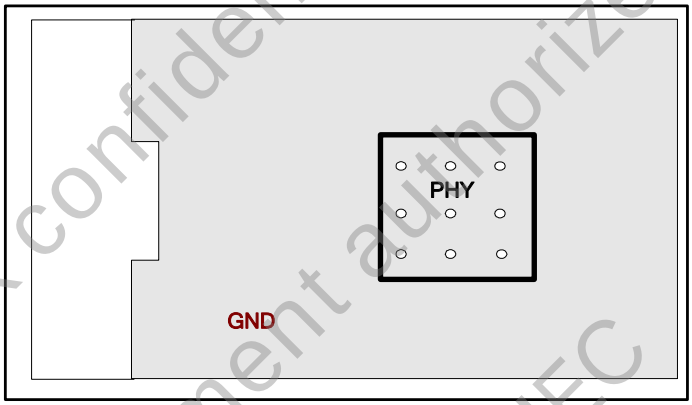

Figure 20. Ground Plane Layout-1

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To achieve better ground plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 21 illustrates a not so good (left) and a good ground plane layout (right).

Figure 21. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 22).

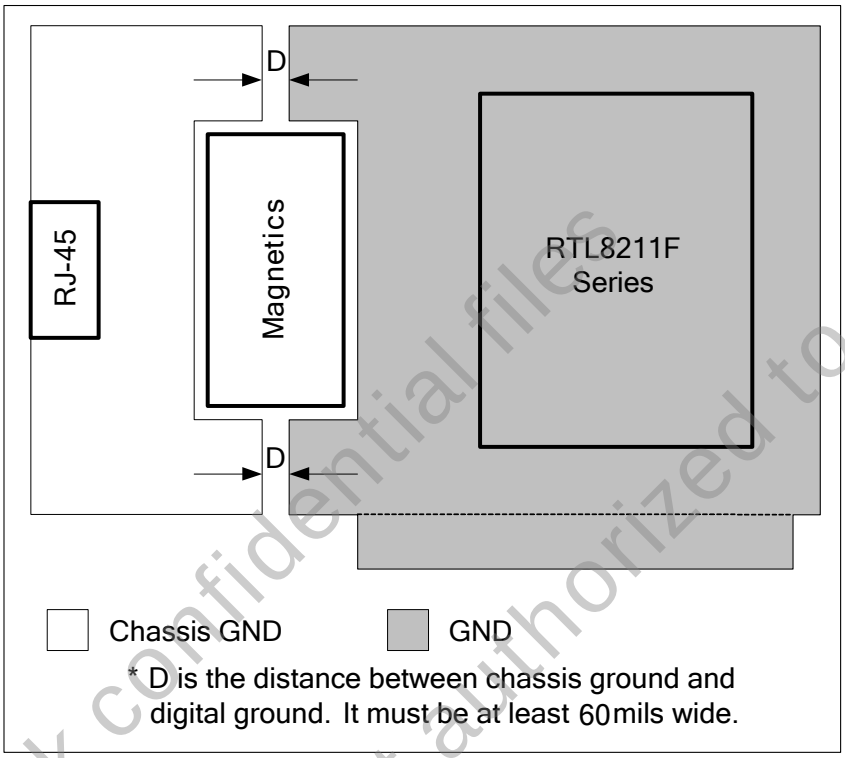

Figure 22. Ground Plane Separation

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The Chassis Ground as shown in Figure 22 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is important to keep the gap (D in Figure 22) between Chassis GND and System GND wider than 60 mils for better isolation.

5.1. Four-Layer Board Ground Plane Layout (Typical Application)

1. Signal 1 (top layer)

2. Power (Keep GND area for RTL8211F PHY)

3. GND

4. Signal 2 (bottom)

5.1.1. Ground Plane Layer 1 Layout

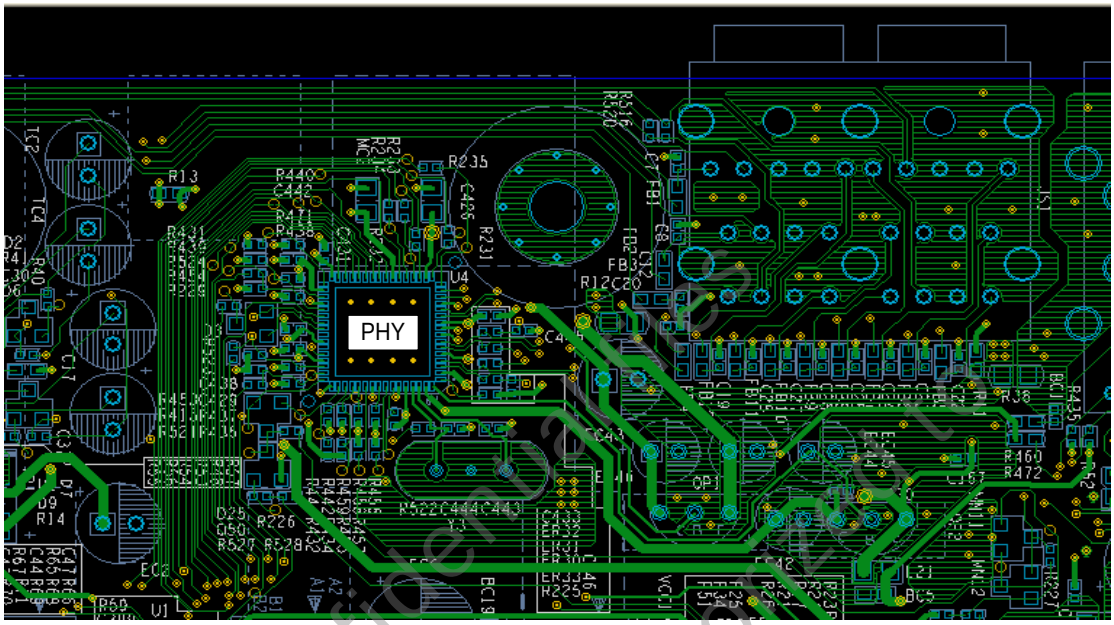

Figure 23. Ground Plane Layer 1 Layout

5.1.2. Ground Plane Layer 2 Layout

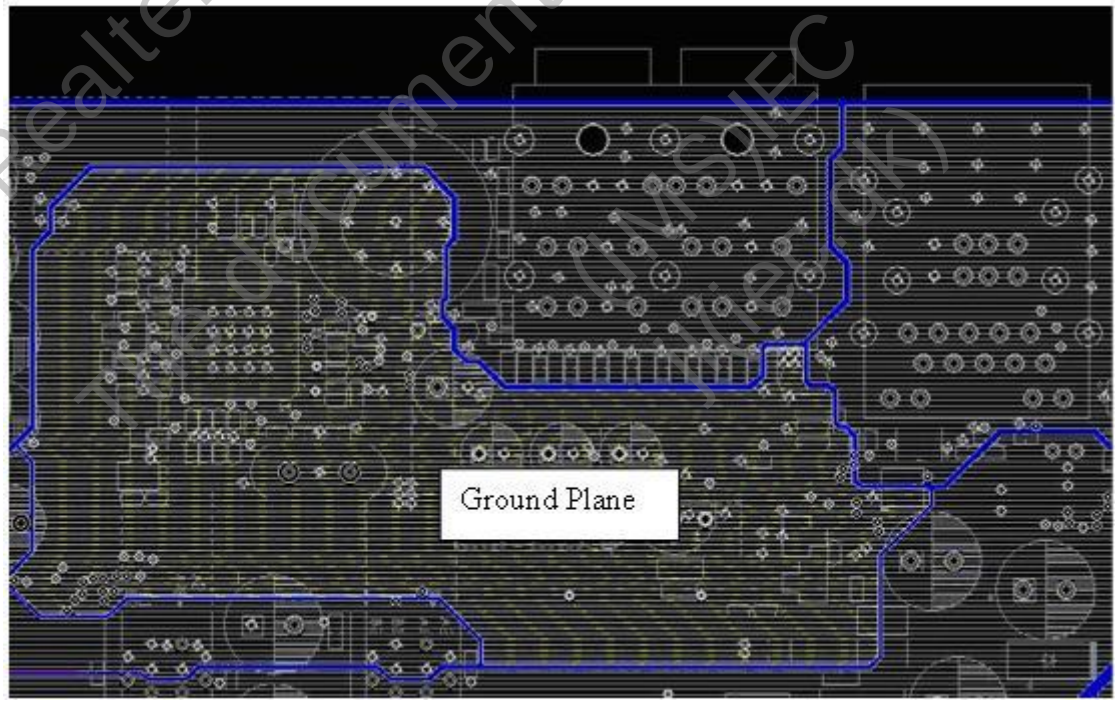

Figure 24. Ground Plane Layer 2 Layout

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5.1.3. Ground Plane Layer 3 Layout

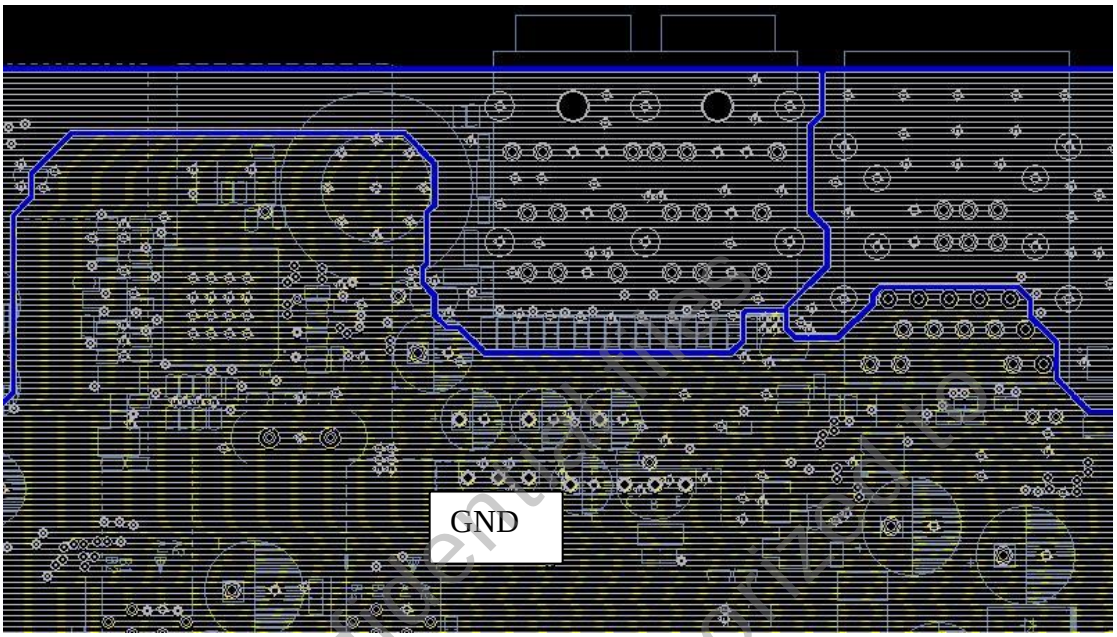

Figure 25. Ground Plane Layer 3 Layout

5.1.4. Ground Plane Layer 4 Layout

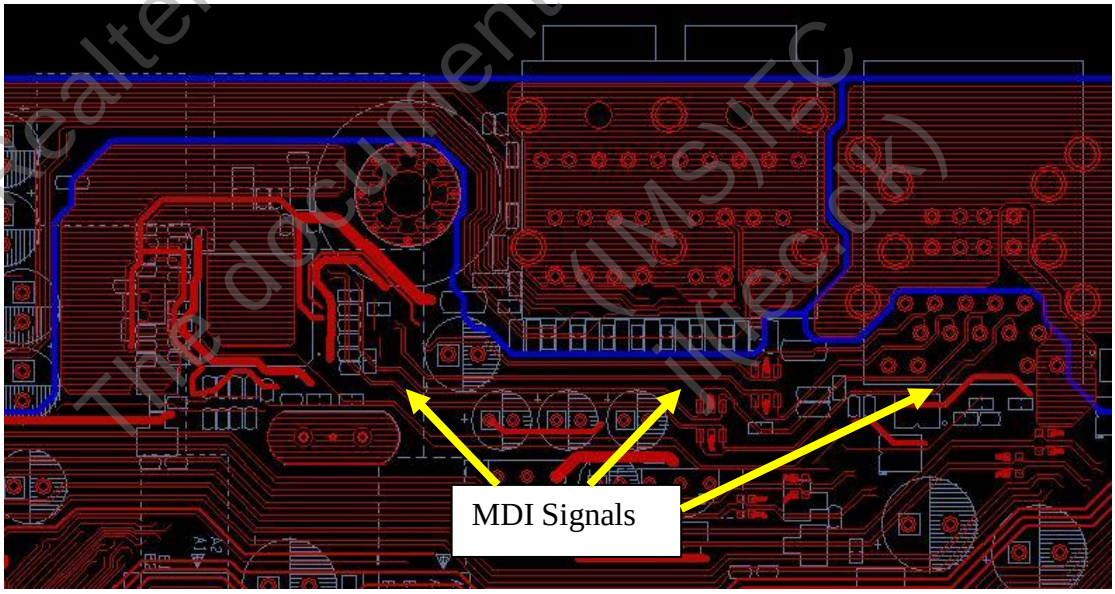

Figure 26. Ground Plane Layer 4 Layout

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6. Power Plane Layout

We recommend using at least a 4-layer PCB. The digital power plane should be separated from analog areas, which are extremely sensitive to noise.

Any analog circuitry on the same plane as the digital power will experience an energy fluctuation due to the fast switching time of digital components. This could improperly bias transistors, and cause the circuits to malfunction. A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration (Figure 27). Keep power traces to the RTL8211F PHY as short and wide as possible and make good use of vias.

(a) Keep the Digital Power Plane as a whole, and leave some space for the Analog Power Plane

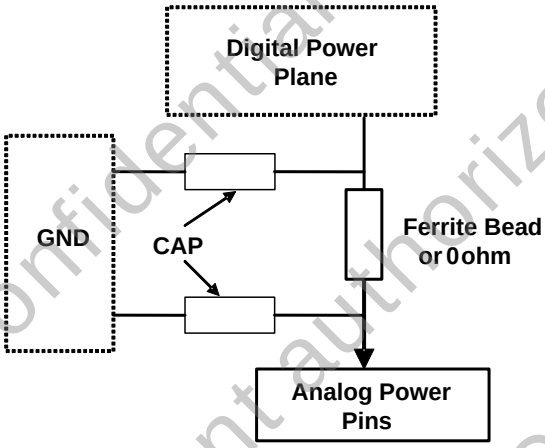

Figure 27. Power Plane

(b) Decoupled Capacitor Example

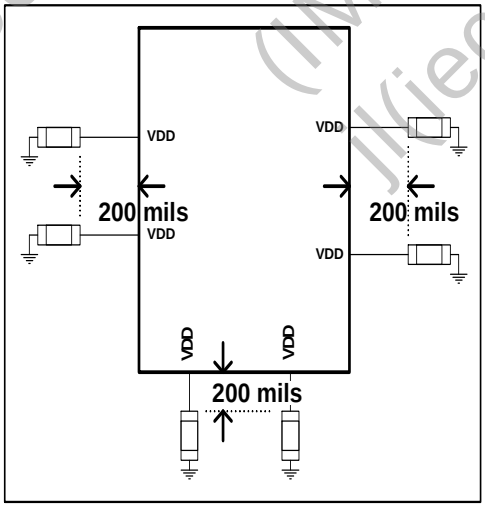

Figure 28. Decoupled Capacitor Example

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To improve the performance of the power plane, try to keep the contact area between the RTL8211F series VDD pins and power plane as large as possible rather than using small narrow traces (Figure 29).

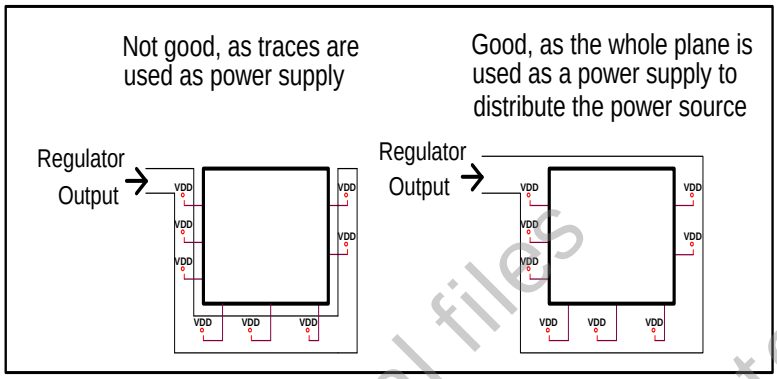

Figure 29. Power Source Distribution

- The 3.3V and 0.9/1.0V power noise levels must be kept below 100mV in gigabit mode.
- All 3.3V and 0.9/1.0V decoupling capacitors shown in the reference schematic (available from Realtek) should be used in all designs.
- The DVDD33/DVDD_RG power plane must be kept as whole and as large as possible.

6.1. Power Plane Layer 1 Layout

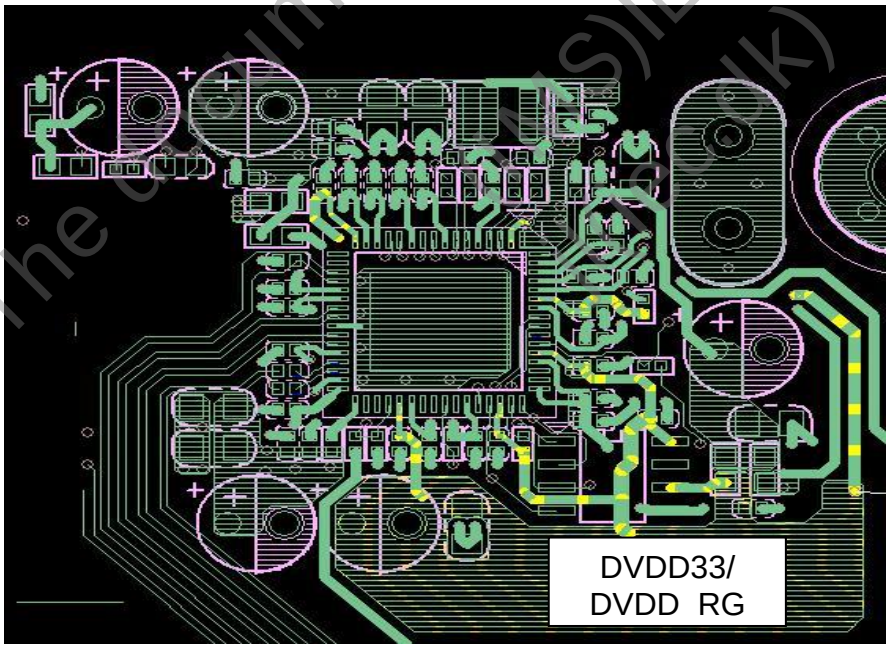

Figure 30. Power Plane Layer 1 Layout

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6.2. Power Plane Layer 4 Layout

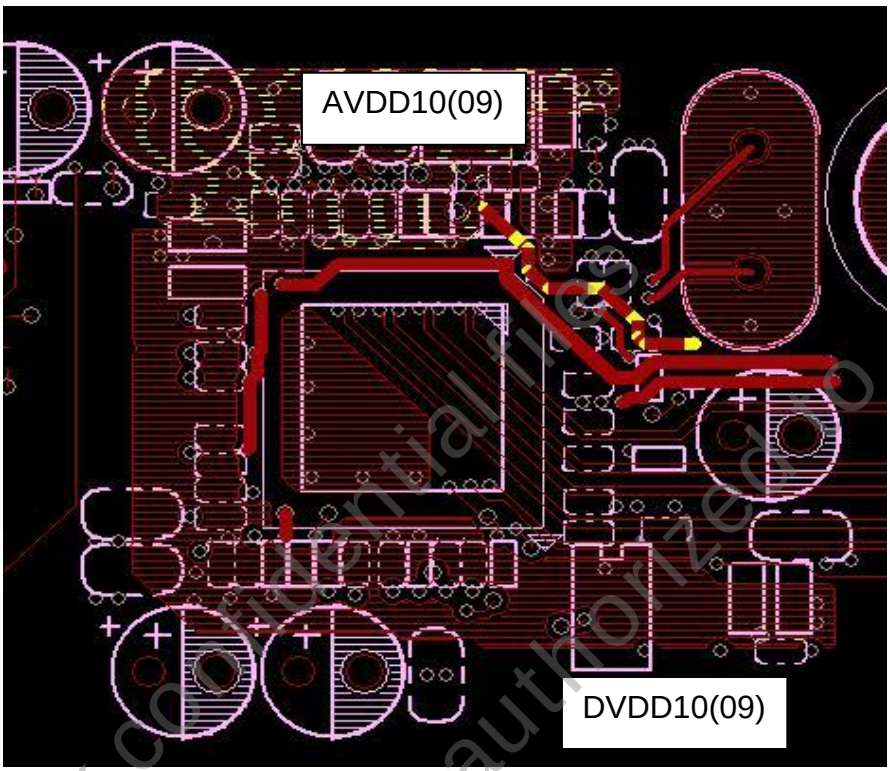

Figure 31. Power Plane Layer 4 Layout

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7. Center-Tapping

- A center-tapped fine-tuned capacitor (Value: 250pF~0.1µF) can improve EMI for single-tone noise.

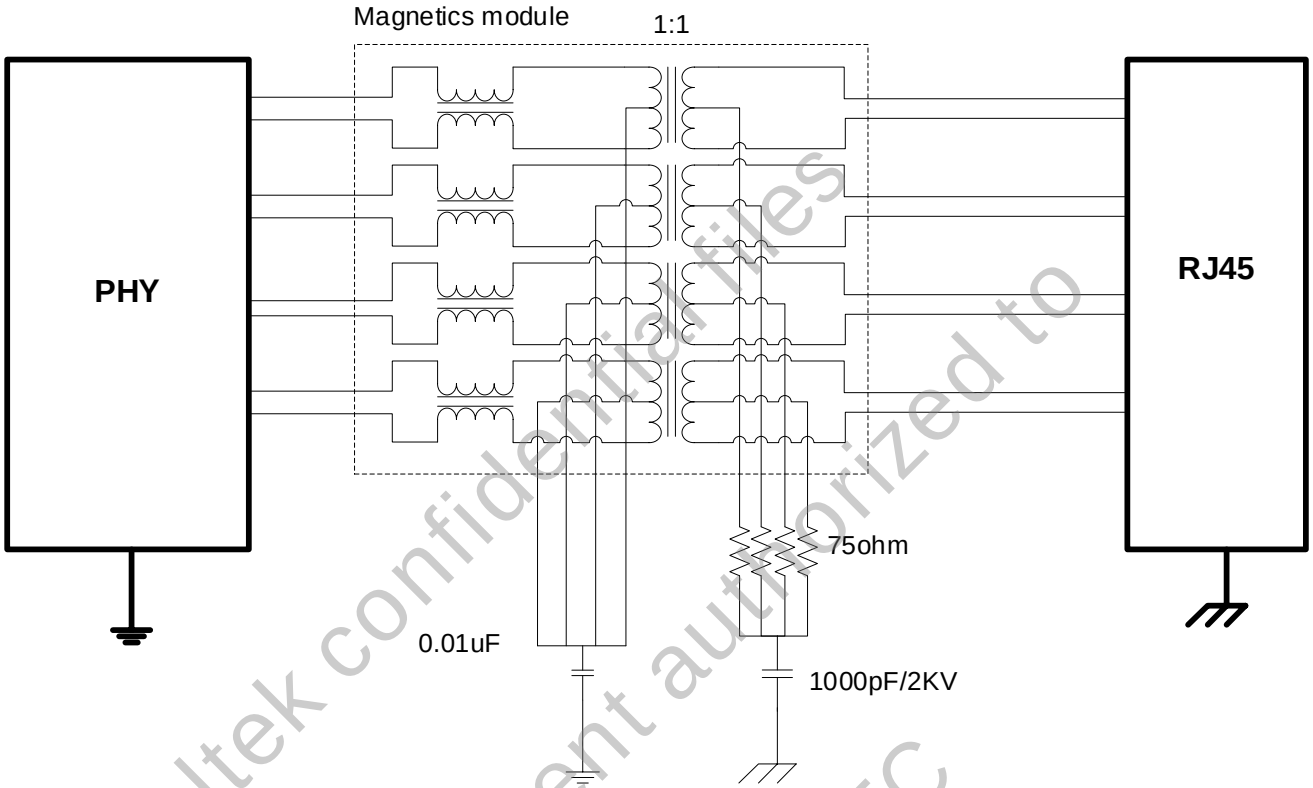

Figure 32. Center-Tapping

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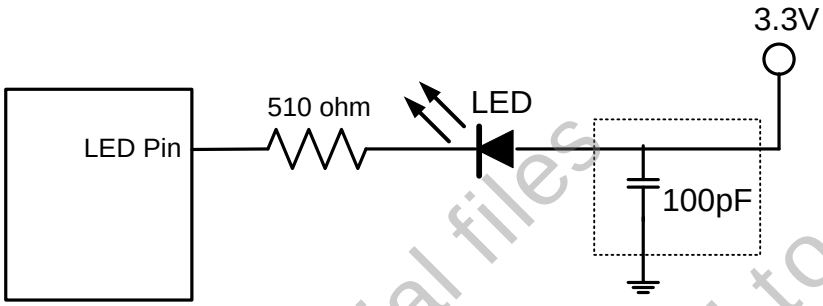
8. LED Pins

- Reserve a decoupling capacitor (D-CAP) for LED pins, and place close to the LAN connector (Refer to the reference schematic, available from Realtek).



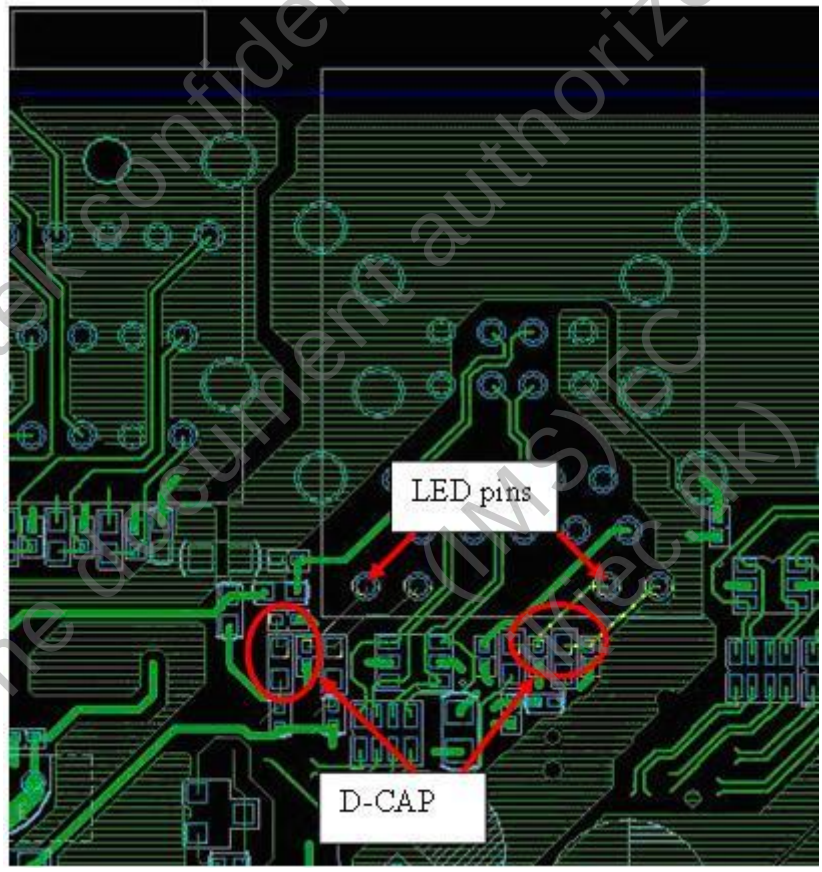


Figure 33. LED Pins

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9. Common Mode Choke

A common mode choke can block common mode noise from the MDI pins. We recommend the value of the common mode choke is 90~120ohm.

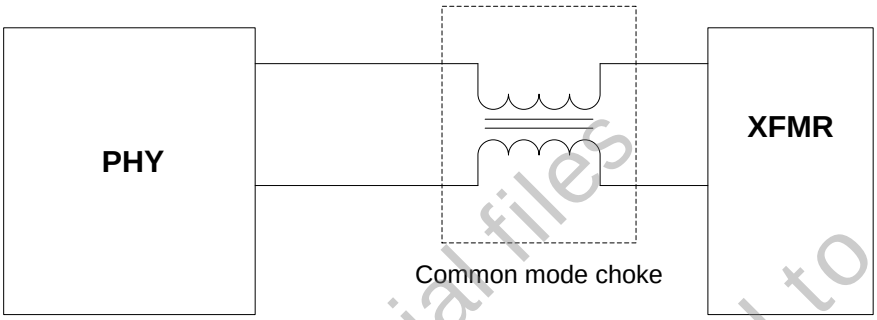

Figure 34. Common Mode Choke

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10. Switching Regulator

The RTL8211F series (except for the RTL8211FD(I)(-VD), which integrates an LDO instead) incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The 0.9/1.0V switching regulator output pin (REG_OUT) should be connected only to DVDD10(09) and AVDD10(09) (do not provide this power source to other devices).

10.1. PCB Layout

- The input 3.3V power trace connected to VDDREG (DVDD33 for RTL8211F(I)(-VD)) must be wider than 40 mils.
- The bulk de-coupling capacitors (Cin1 and Cin2) must be placed within 200 mils (0.5cm) of VDDREG (DVDD33 for RTL8211F(I)(-VD)) to prevent input voltage overshoot.
- The output power trace of REG_OUT must be wider than 60 mils.
- Lx (2.2µH) must be kept within 200 mils (0.5cm) of REG_OUT.
- Cout1 and Cout2 must be kept within 200 mils (0.5cm) of Lx to ensure stable output power and better power efficiency.
- For switching regulator stability, the capacitors Cout1 and Cout2 must be ceramic (X5R/X7R) capacitors, the footprint of the capacitors must be 0603 size minimum, or over. Any inductance or bead, except for Lx, is not allowed on the path from REG_OUT to DVDD10(09)/AVDD10(09).
- Cin1 and Cin2 are also recommended to be ceramic (X5R/X7R) capacitors, and the footprint of the capacitors also must be 0603 size at least.
- Place Lx and Cin1 on the same layer as the RTL8211F PHY. Do not use vias on VDDREG (DVDD33 for RTL8211F(I)(-VD)) and REGOUT traces.
- The total caps value of 0.9/1.0V trace is 4.7~11uF(X5R).

Note: Violation of the above rules will damage the IC.

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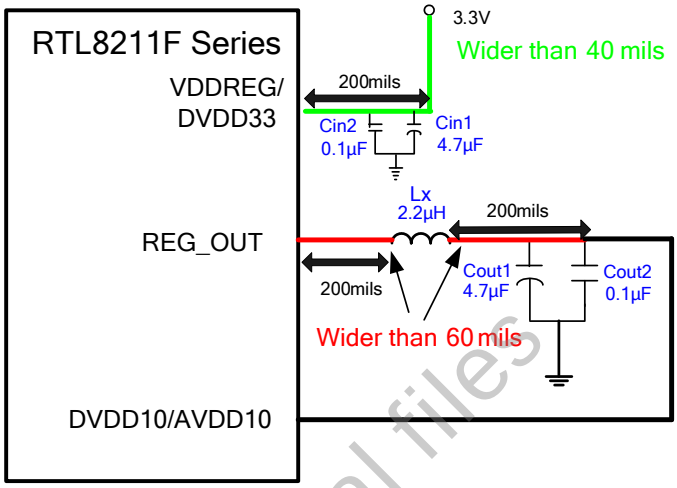

Figure 35. Switching Regulator

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11. Low-Dropout Regulator (RTL8211FD(I)(-VD) Only)

The RTL8211FD(I)(-VD) incorporates a linear low-dropout regulator (LDO) that features high power supply ripple rejection and low output noise. A power inductor is not needed for the RTL8211FD(I)(-VD); only an output capacitor is required between the 0.9/1.0V output and the analog ground for phase compensation, which saves cost and PCB real estate.

Use an X5R/X7R low-ESR ceramic capacitor, with capacitance of at least 0.1µF, to enhance the stability of the output voltage. The bypass capacitors should be placed as close as possible to power pins (AVDD10(09) and DVDD10(09)) for adequate filtering.

The regulator 0.9/1.0V output pin (LDO_OUT) should be connected only to DVDD10(09) and AVDD10(09) pins (do not provide this power source to other devices).

Note: With respect to the voltage conversion efficiency, an LDO is inferior to a switching regulator. The trade-off between BOM cost, size, and efficiency should all be taken into account when choosing the regulator type.

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12. Parts Recommendations

12.1. 10/100/1000M Magnetic

Turn Ratio TX/RX: 1:1

Primary Inductance: 350µH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature:

0°C to 70°C for RTL8211F(D)/RTL8211FS(-VS)/RTL8211FG(-VS)

-40°C to 85°C for RTL8211F(D)I/RTL8211FSI(-VS)/RTL8211FGI(-VS)

Recommended Magnetics: Pulse H5007 or similar

12.2. Resistors

Resistors that have tolerance requirements within 1% are strongly recommended. See the reference schematic (available from Realtek) for details.

12.3. Capacitors

For switching regulator power filtering, an X5R/X7R ceramic capacitor is recommended for the power circuit.

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12.4. Power Inductor

The power inductor used by the switching regulator must be capable of handling 600mA of current. The variance in the inductance value should be less than 20% under 600mA of current. The resistance value should be as small as possible to achieve the expected switching regulator efficiency, which must be higher than 75%.

Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%.

12.5. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

13. Special Notes

- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions.
- The GMII/RGMII traces are high-speed signal traces. For the best performance, be sure to follow all GMII/RGMII-specific layout guidelines.

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